InGaSb p-Channel Self-Aligned FinFETs with 10 nm Fin-Width Using Sb-Compatible Digital Etch

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Sponsors:
DTRA
KIST
Lam Research
SRC

Outline

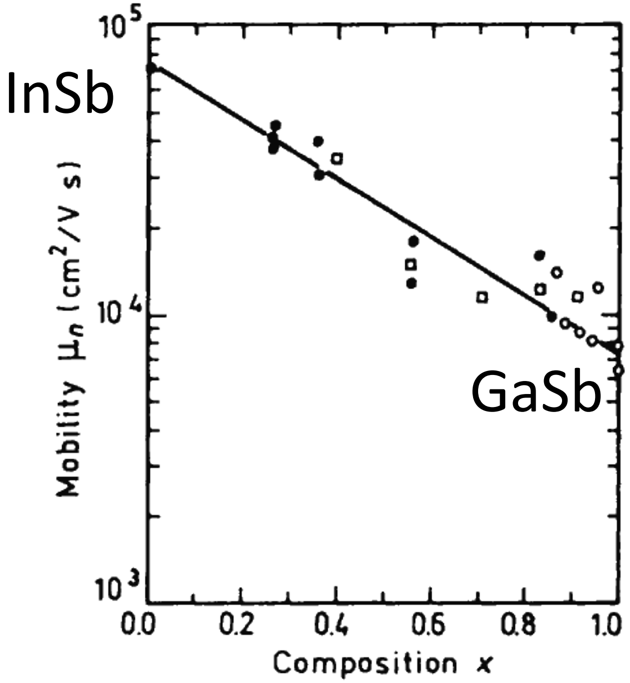
- Motivation
- Key technology: III-Sb-compatible digital etch
- InGaSb p-channel FinFET fabrication
- Electrical characteristics
- Conclusions

A Case for III-Sb

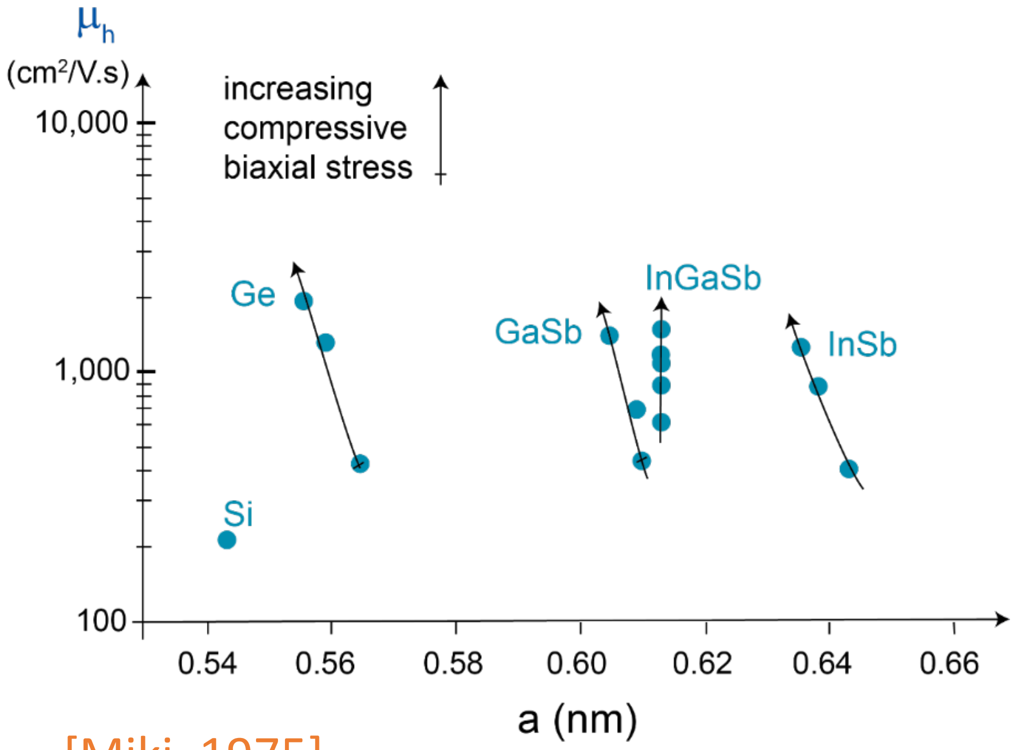
Properties of III-Sb:

- High μ_n
- High μ_p
- Strong strain effect
- E_g engineering
- Applications in photonics, etc.

Electron mobility

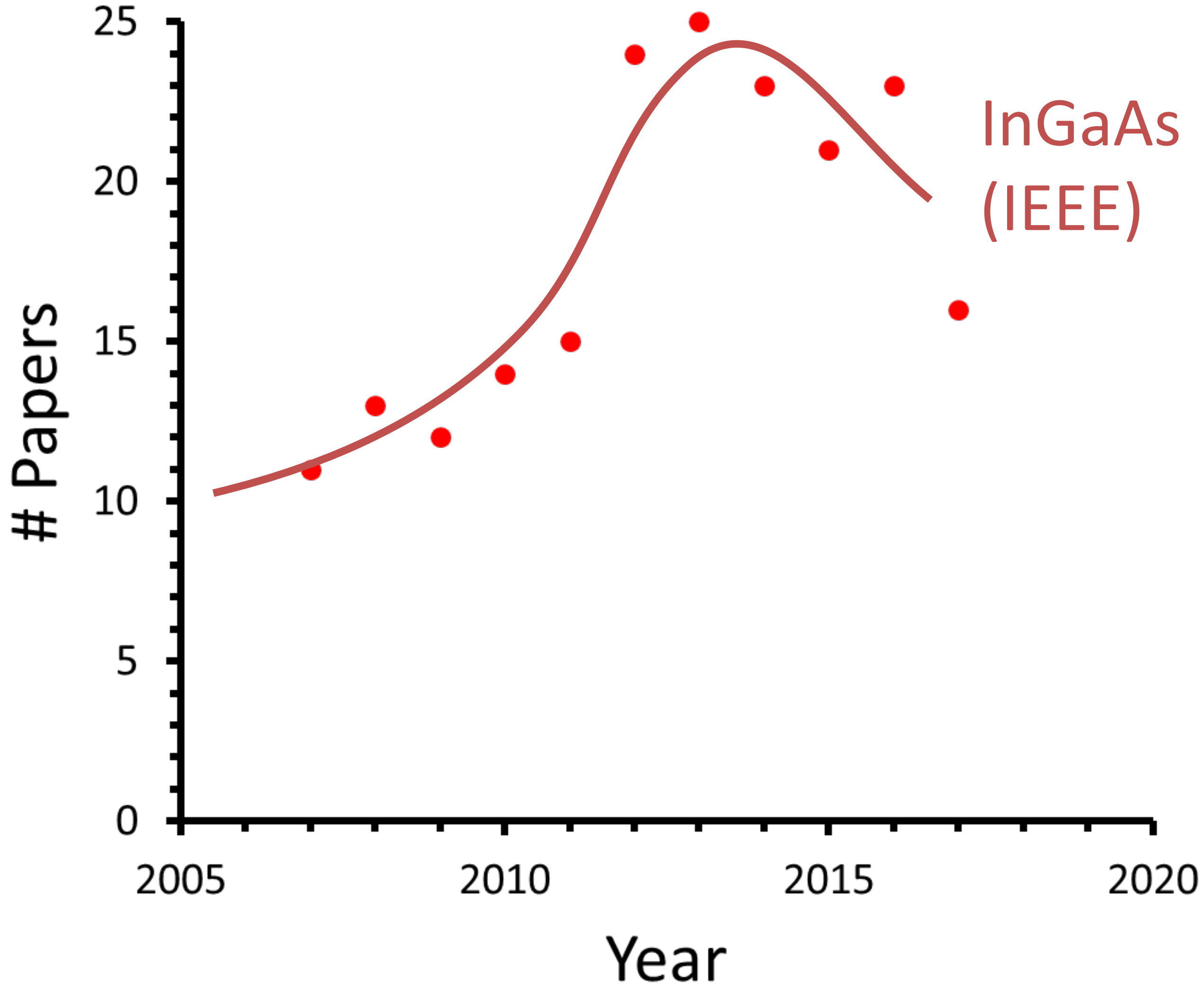


Hole mobility in QW-FETs

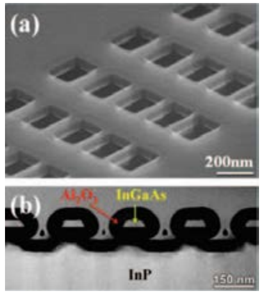


[Miki, 1975]
[Kawashima and Kataoka, JJAP 1979]
[del Alamo, Nature, 2011]

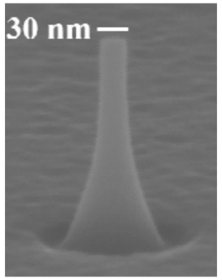
III-Sb Transistor Research



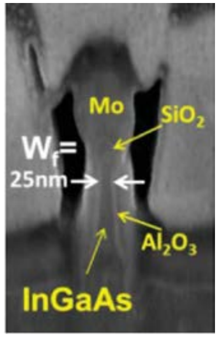
III-Sb Transistor Research



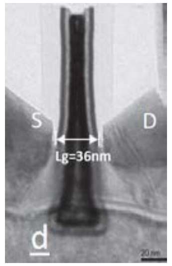
Gu, IEDM 2011



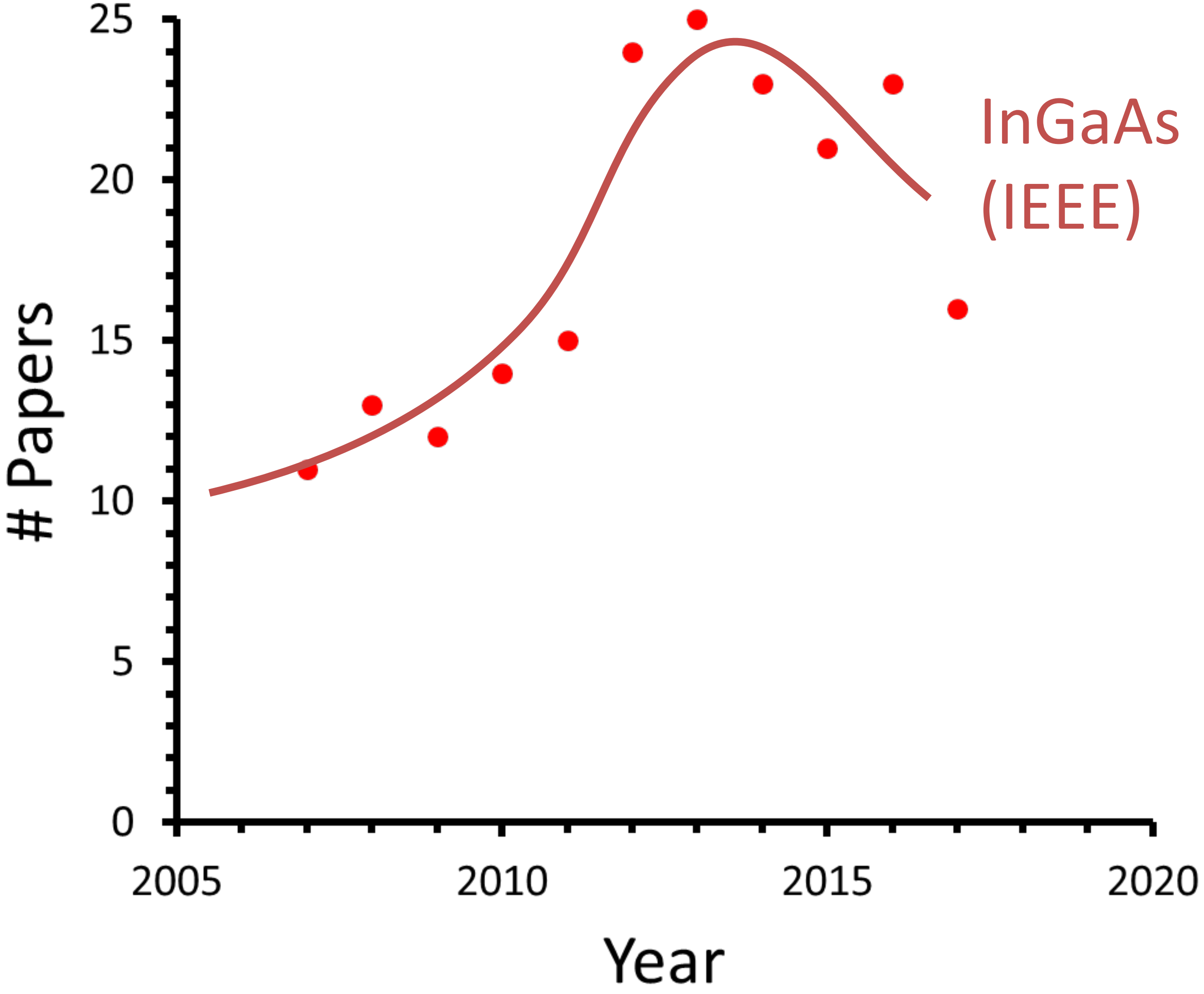
Zhao, IEDM 2013

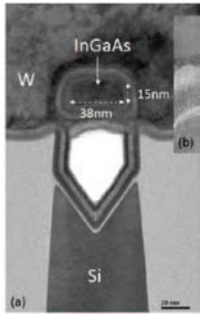


Vardi, IEDM 2015

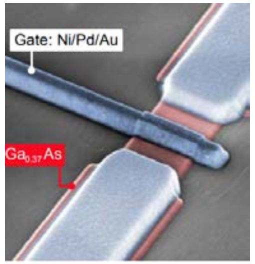


Zhou, VLSI 2016

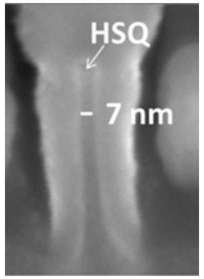




Waldron, VLSI 2016

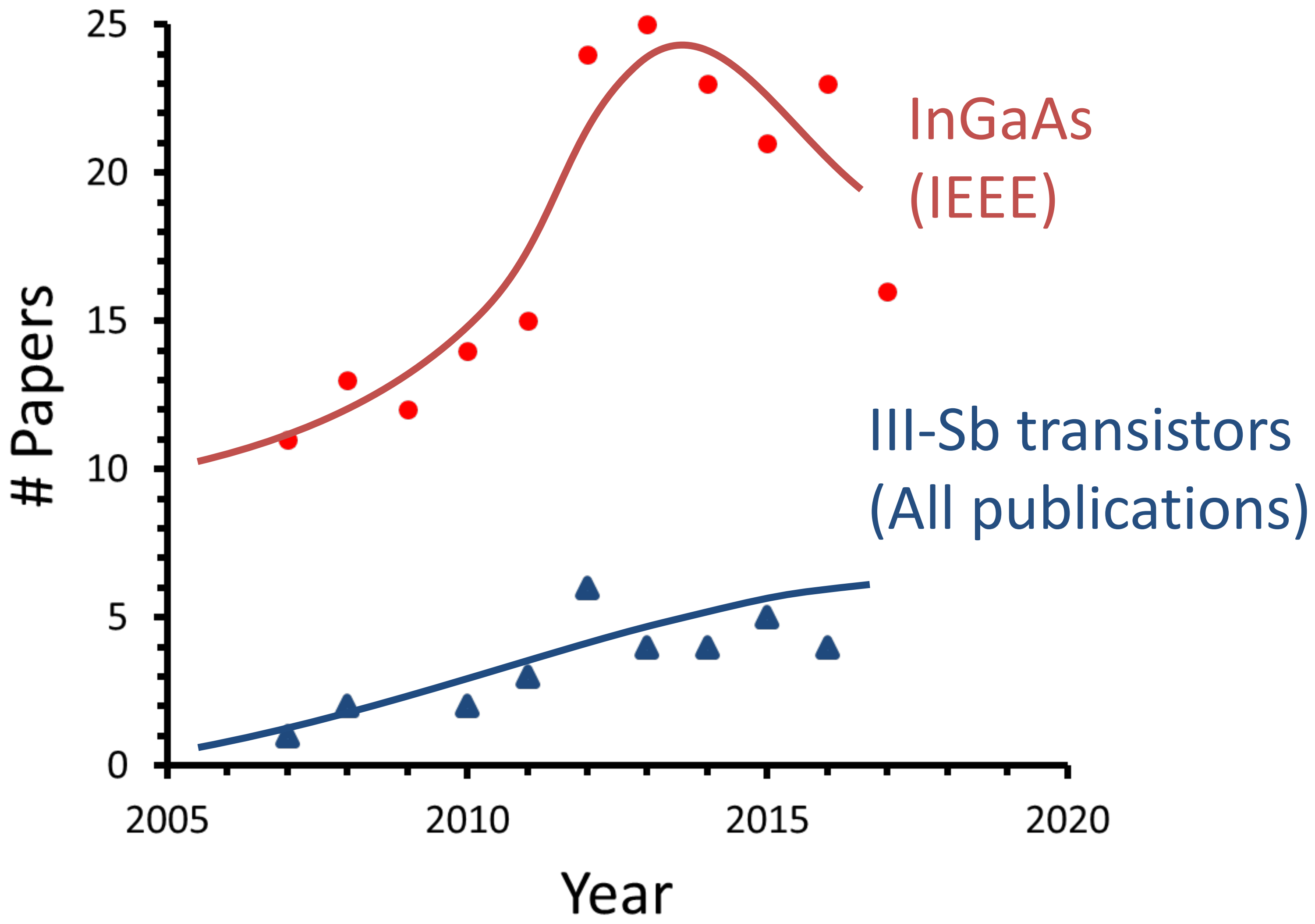


Zota, IEDM 2016

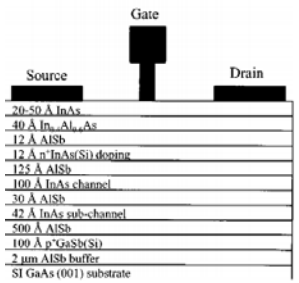


Vardi, EDL 2016

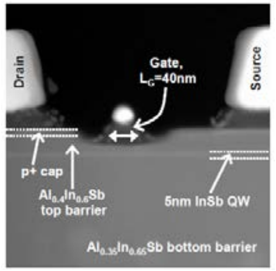
III-Sb Transistor Research



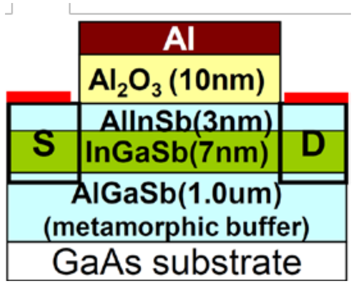
III-Sb Transistor Research



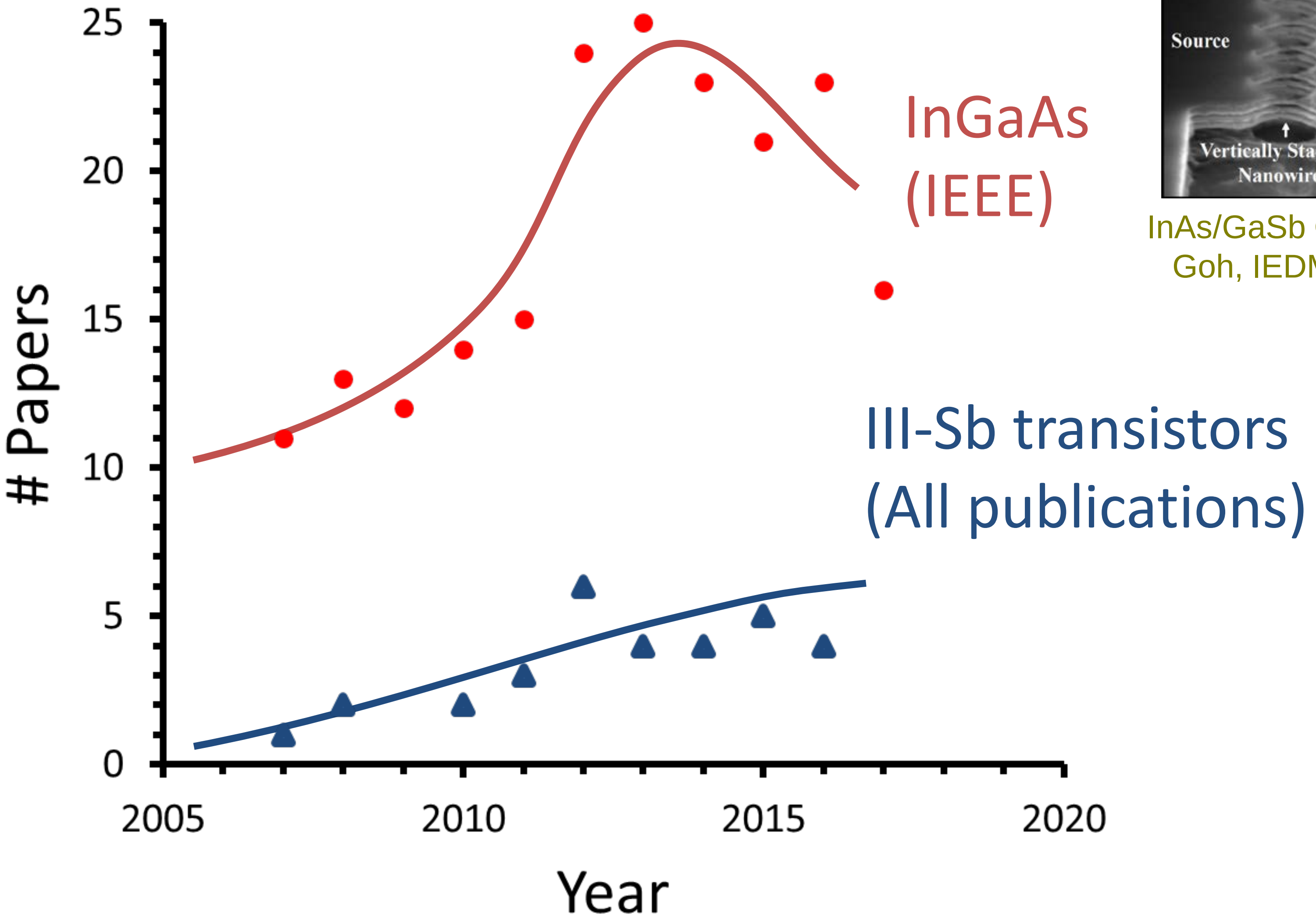
InAs/AlSb/GaSb HEMT
B. Bennett, JVST ’00

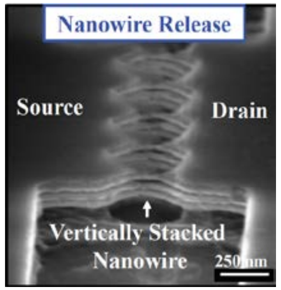


InSb QW p-FET
Radosavljevic, IEDM ’08

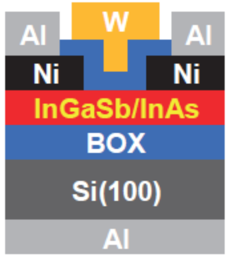


InGaSb p-MOSFET
Nainani, IEDM ’10

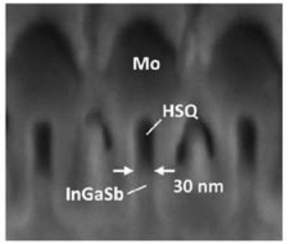




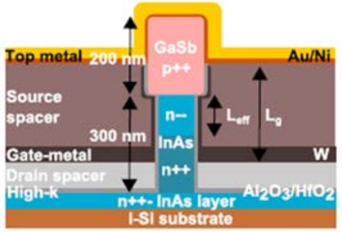
InAs/GaSb CMOS
Goh, IEDM ’15



InGaSb p-SOI
Nishi, VLSI ’15



InGaSb p-FinFET
Lu, IEDM ’15

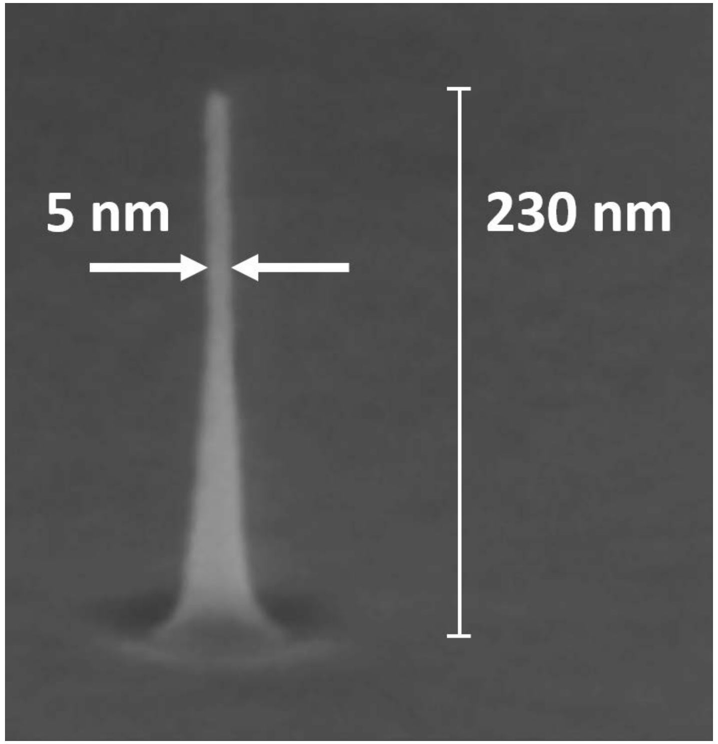


InAs/GaSb TFET
Memišević, EDL ’16

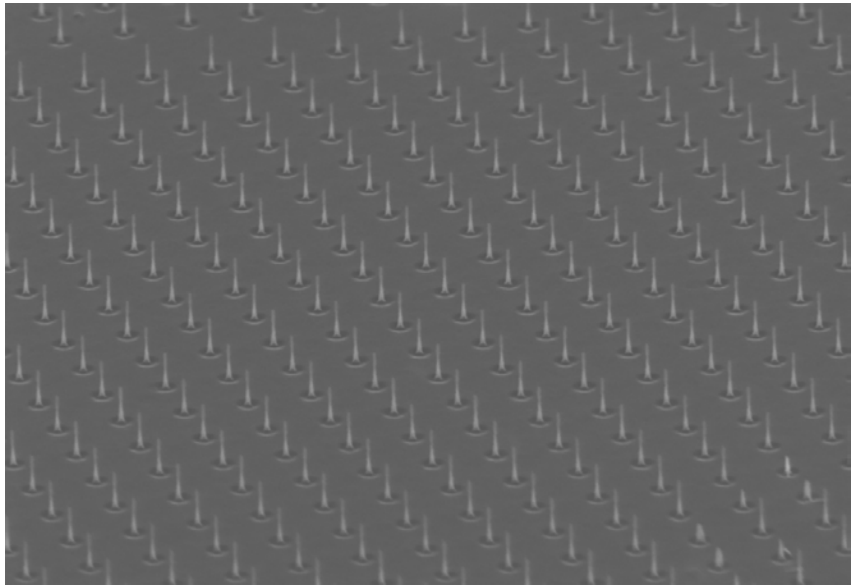
Challenges: III-Sb Digital Etch

W_F = 5 nm

D = 5 nm



D = 8 nm

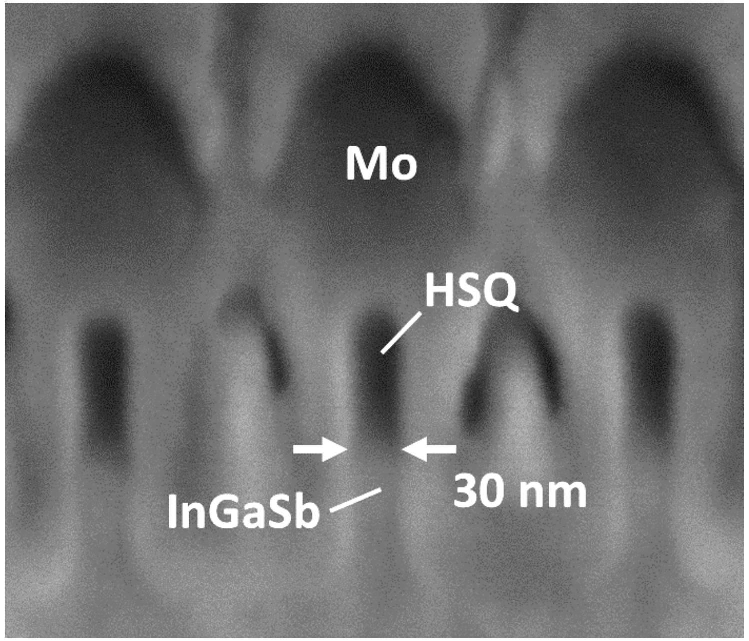


[Vardi, IEDM 2017]
[Lu, EDL, 2017]

Digital etch: key of sub-10 nm InGaAs transistors

Challenges: III-Sb Digital Etch

XSEM of InGaSb FinFET

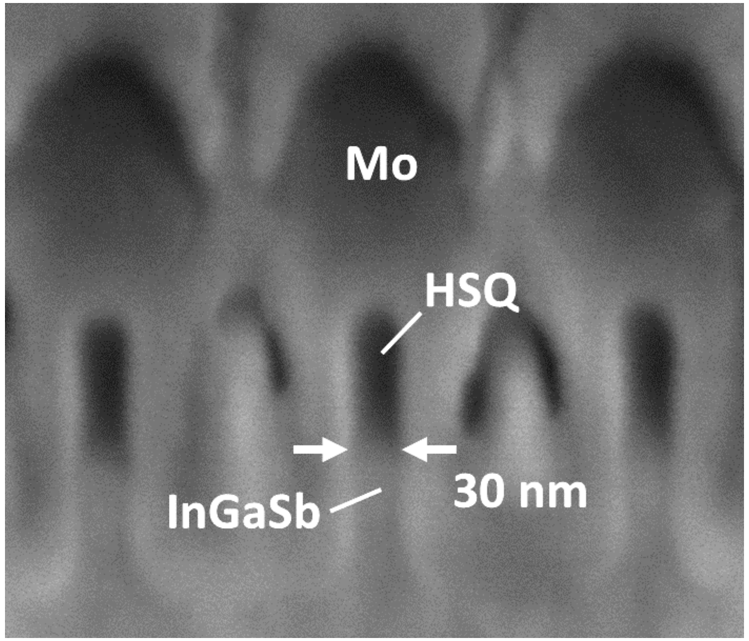


[Lu, IEDM, 2015]

- W_f limited by EBL and RIE

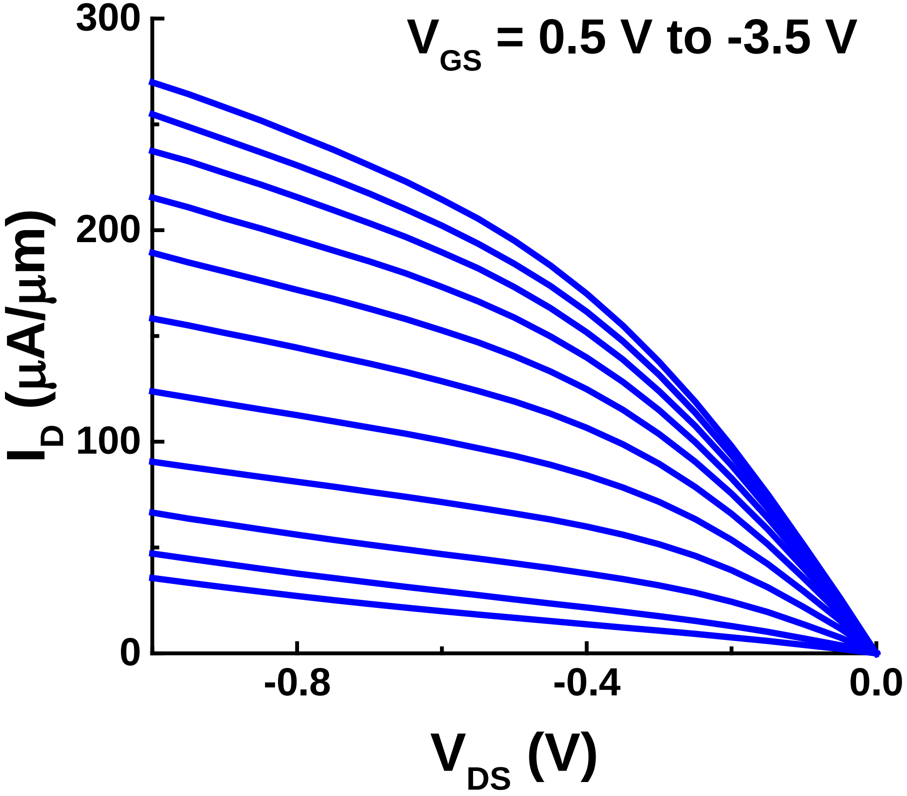
Challenges: III-Sb Digital Etch

XSEM of InGaSb FinFET



[Lu, IEDM, 2015]

W_f = 30 nm, L_g = 100 nm



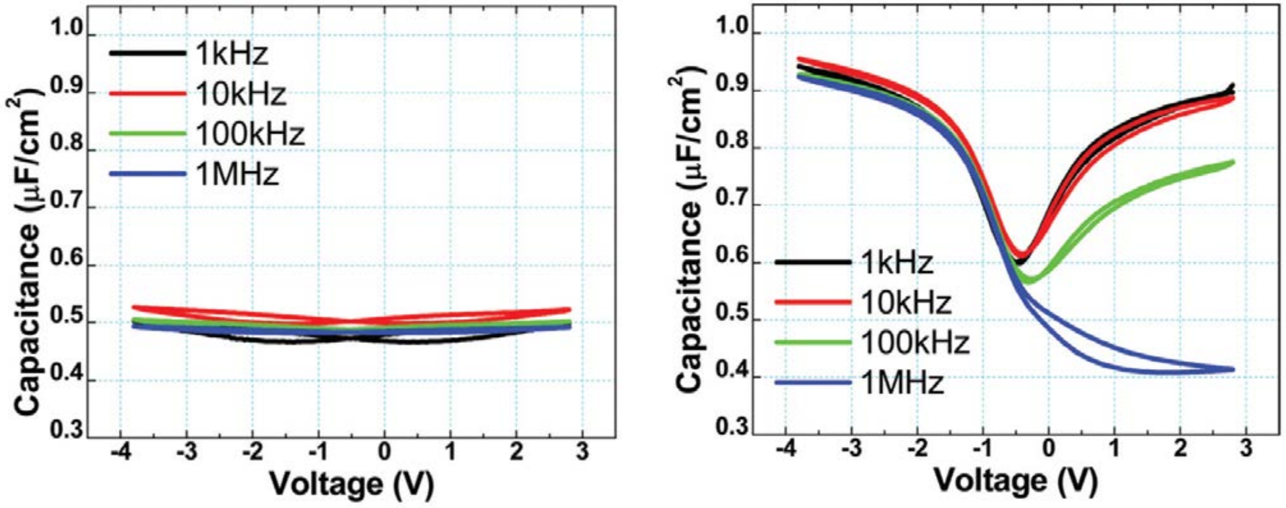
- W_f limited by EBL and RIE
- Suffers from large off current

HCl Digital Etch on III-Sb

- Previous research: HCl cleans GaSb surface

[Nainani, JAP 2011]

GaSb MOSCAPs



As-Is

HCl

HCl Digital Etch on III-Sb

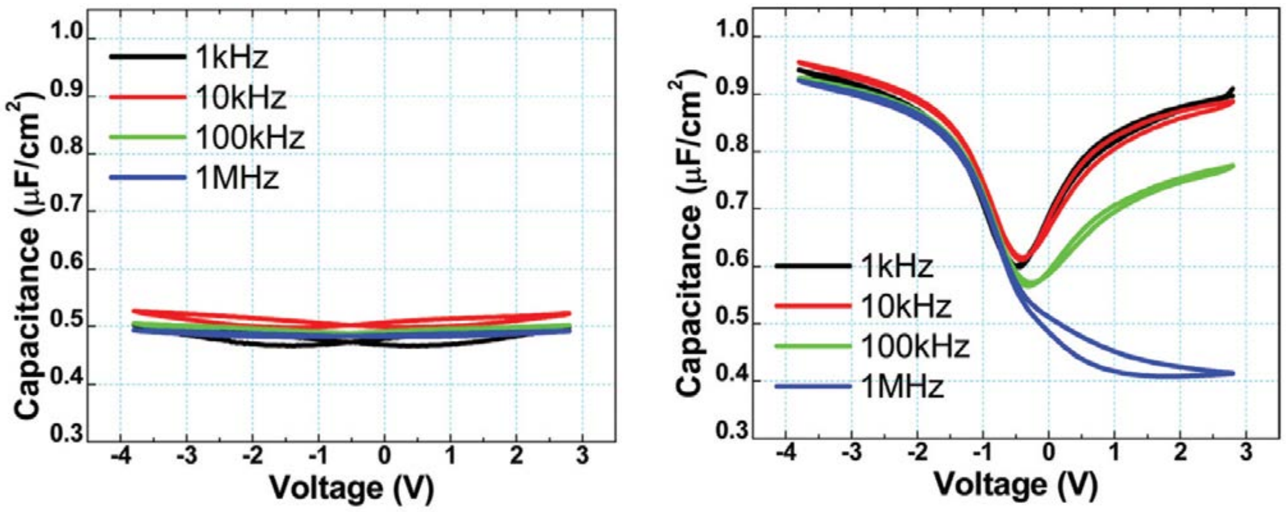
- Previous research: HCl cleans GaSb surface

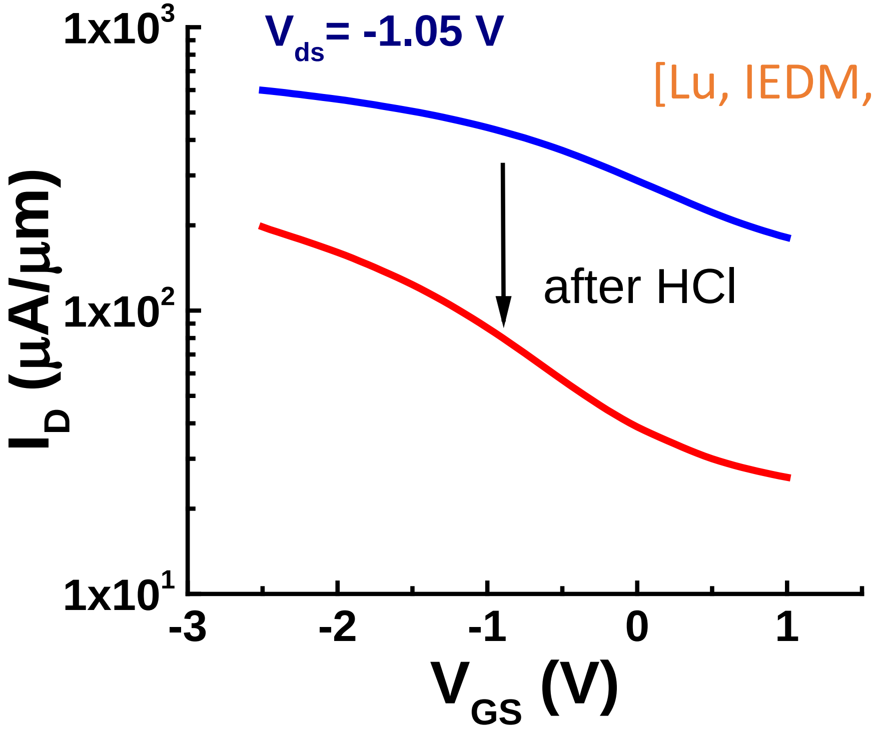
[Nainani, JAP 2011]

GaSb MOSCAPs

As-Is

HCl



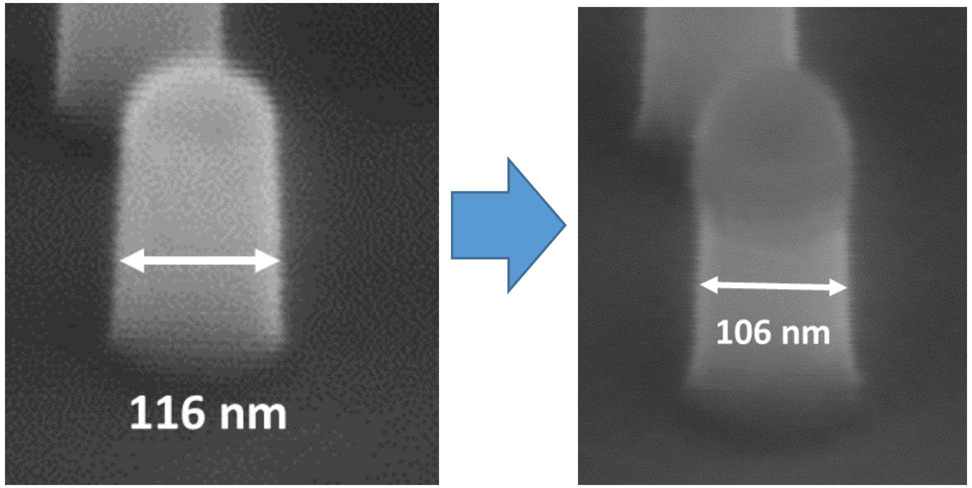


[Lu, IEDM, 2015]

FinFETs: only mild improvement of off current

Issue with HCl Digital Etch

- HCl etches the InGaSb sidewall

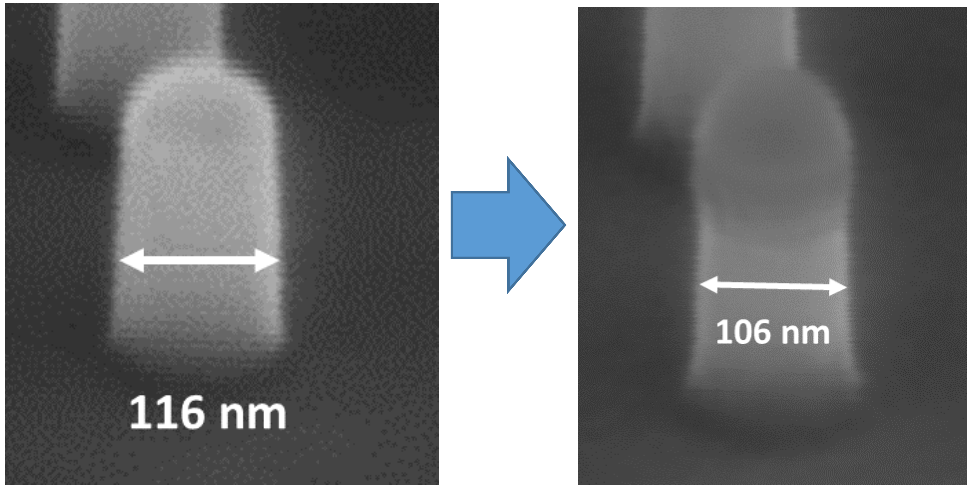

After RIE

1% HCl 30s

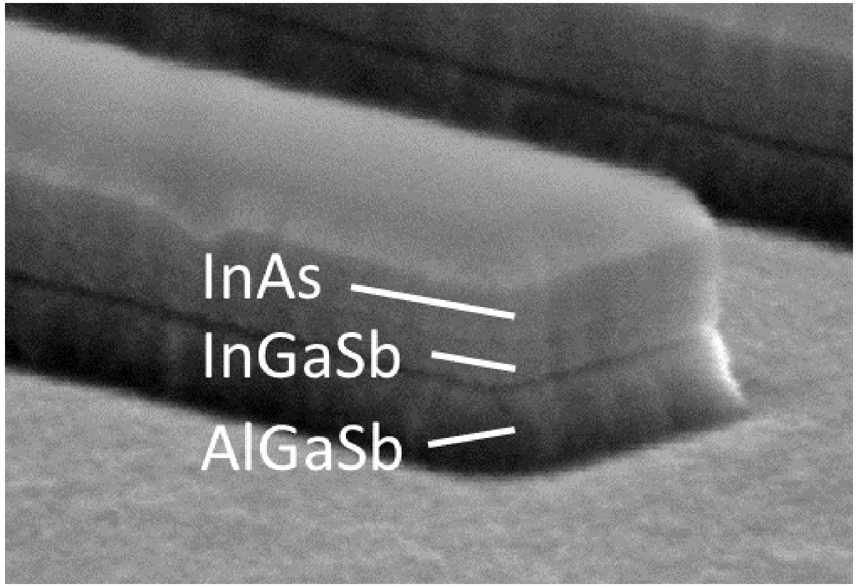
Issue with HCl Digital Etch

- HCl etches the InGaSb sidewall

After RIE 1% HCl 30s

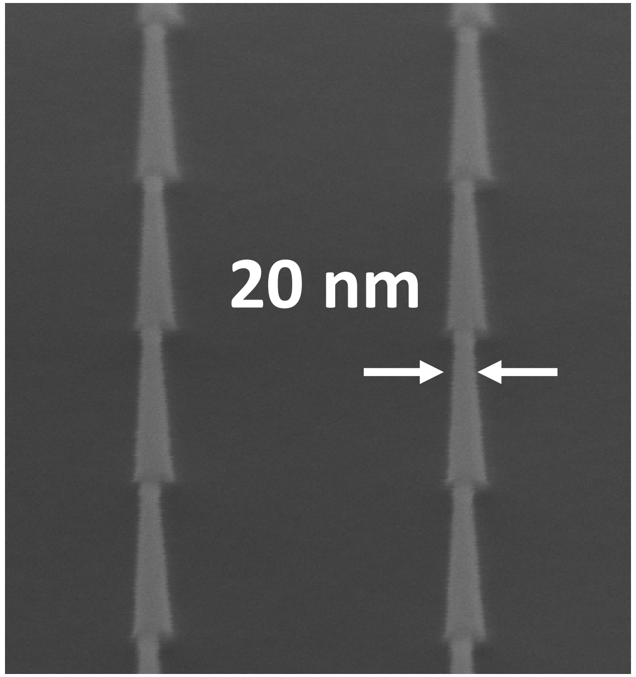


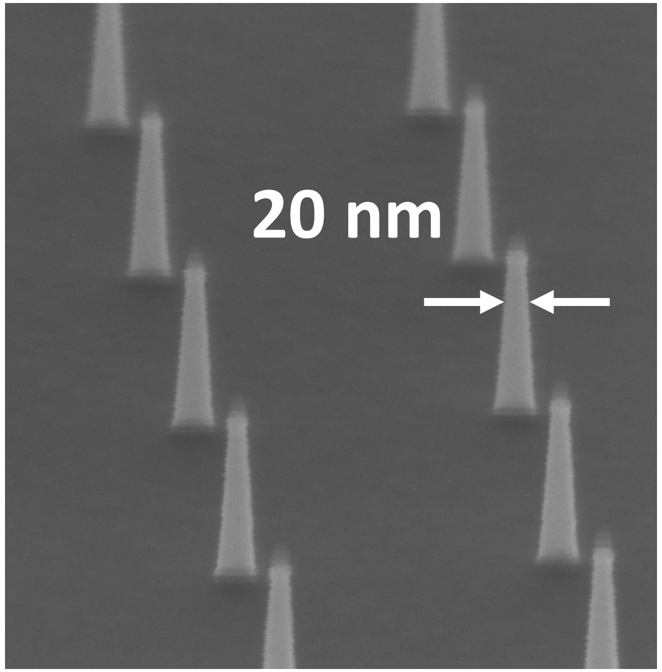
DI water 2 min



Water-based HCl problematic for III-Sb DE

Alcohol-based Digital Etch


After RIE

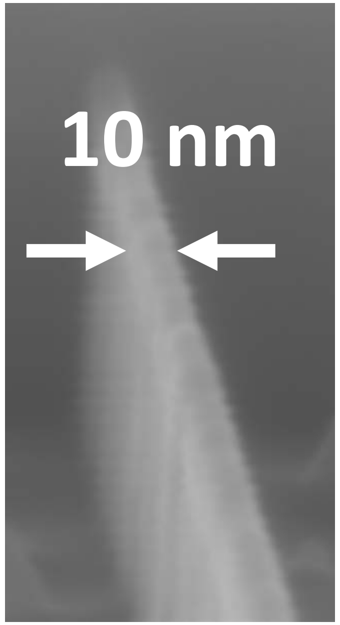

10% HCl:IPA 2 min

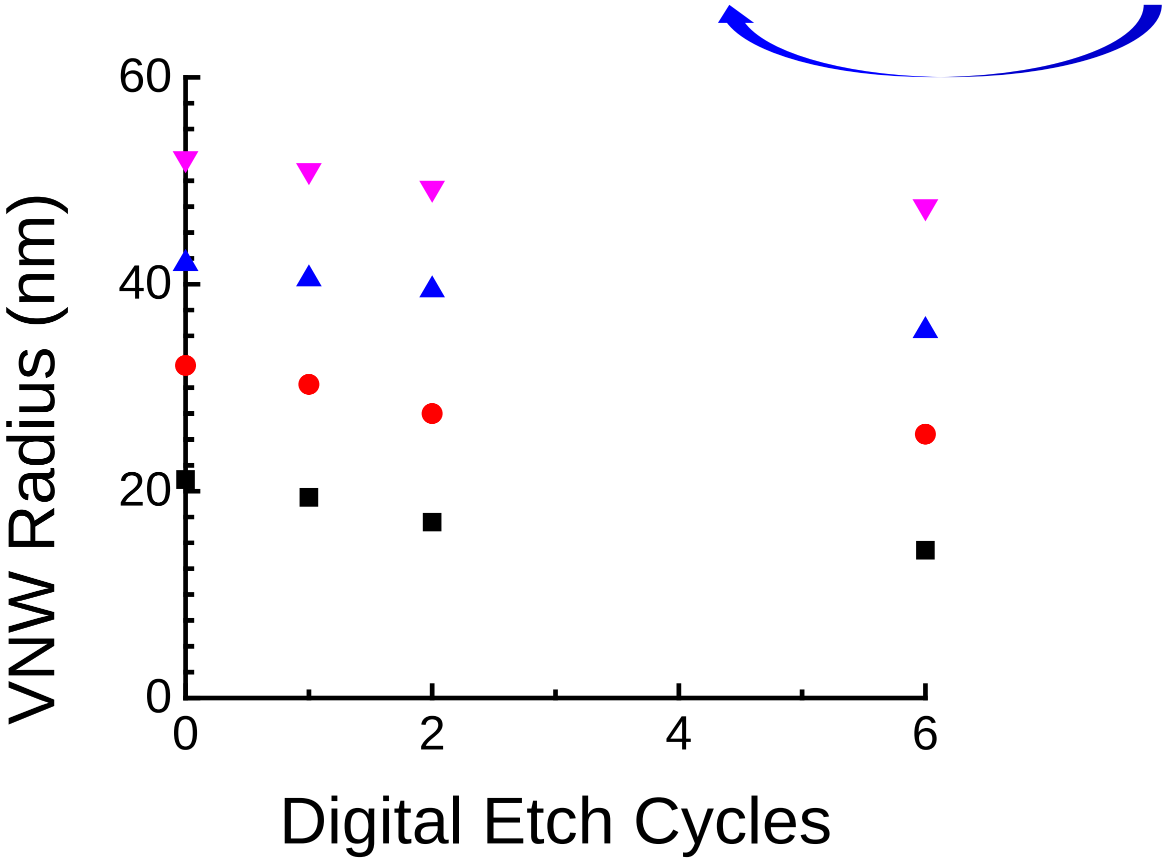
[Lu, EDL, 2017]

- Self-limiting process
- No damage on the sidewall

Alcohol-based Digital Etch

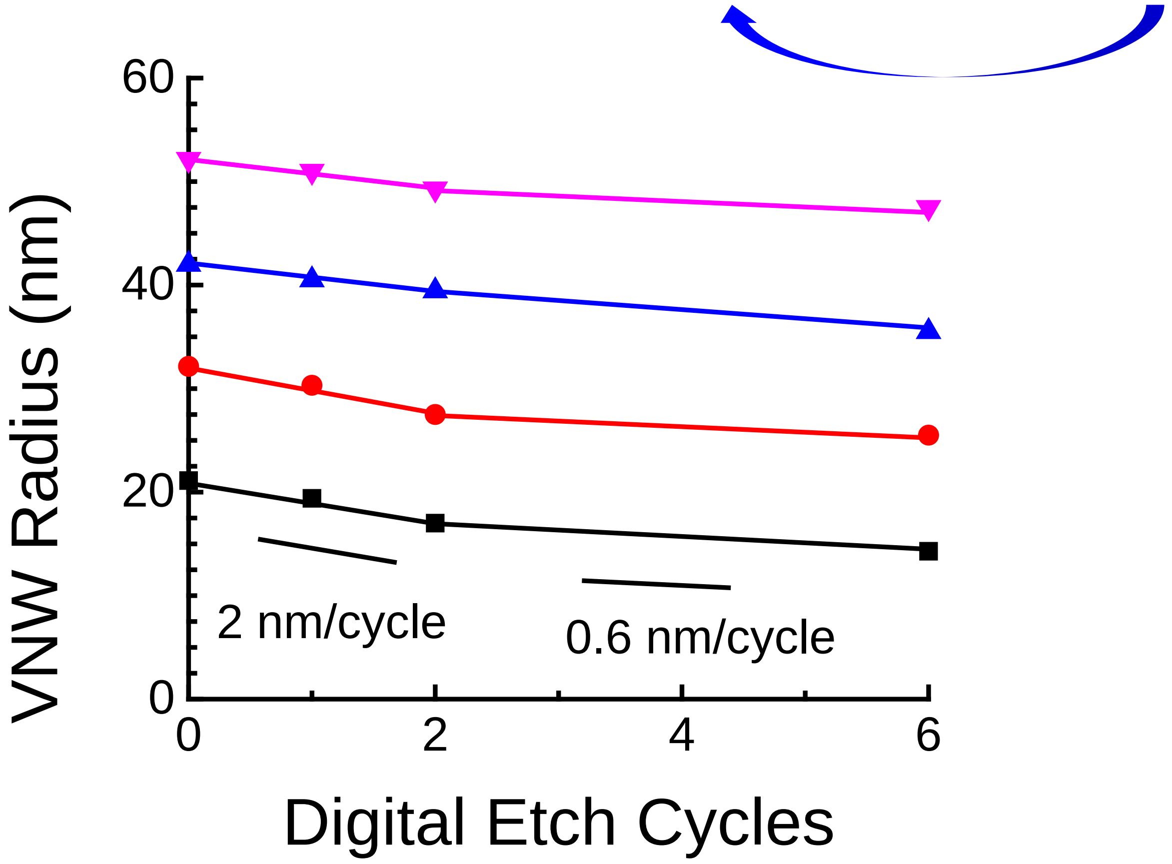
First digital etch on III-Sb: HCl:IPA + O_2 plasma





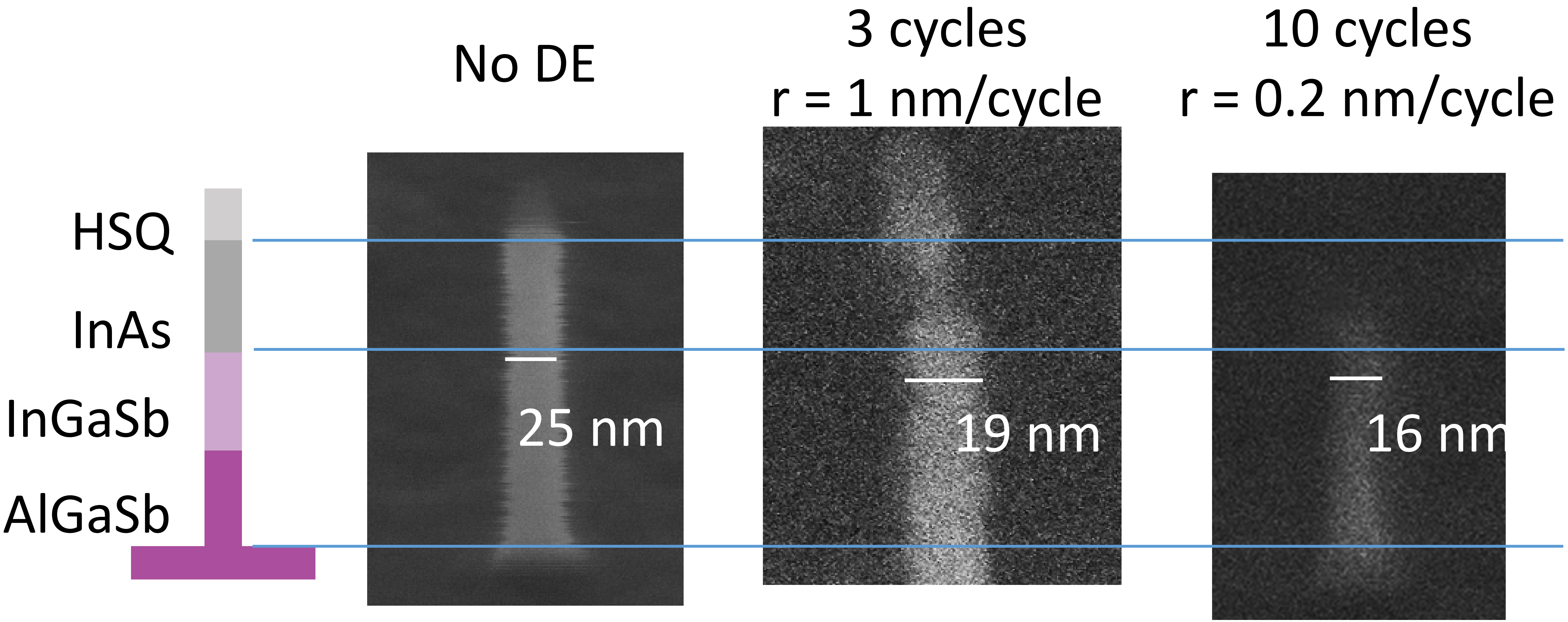
Alcohol-based Digital Etch

First digital etch on III-Sb: HCl:IPA + O_2 plasma



Etch rate ↓ after multiple DE cycles

Alcohol-based Digital Etch



- r (III-Sb) ↓ after 3 cycles
- r (III-As) >> r (III-Sb)

Sb-compatible Digital Etch

Oxidation of GaSb:

- In air:
  - Ga_2O_3, Sb_2O_3

[Liu, JVST B. 2002]

III-Sb-compatible Digital Etch

Oxidation of GaSb:

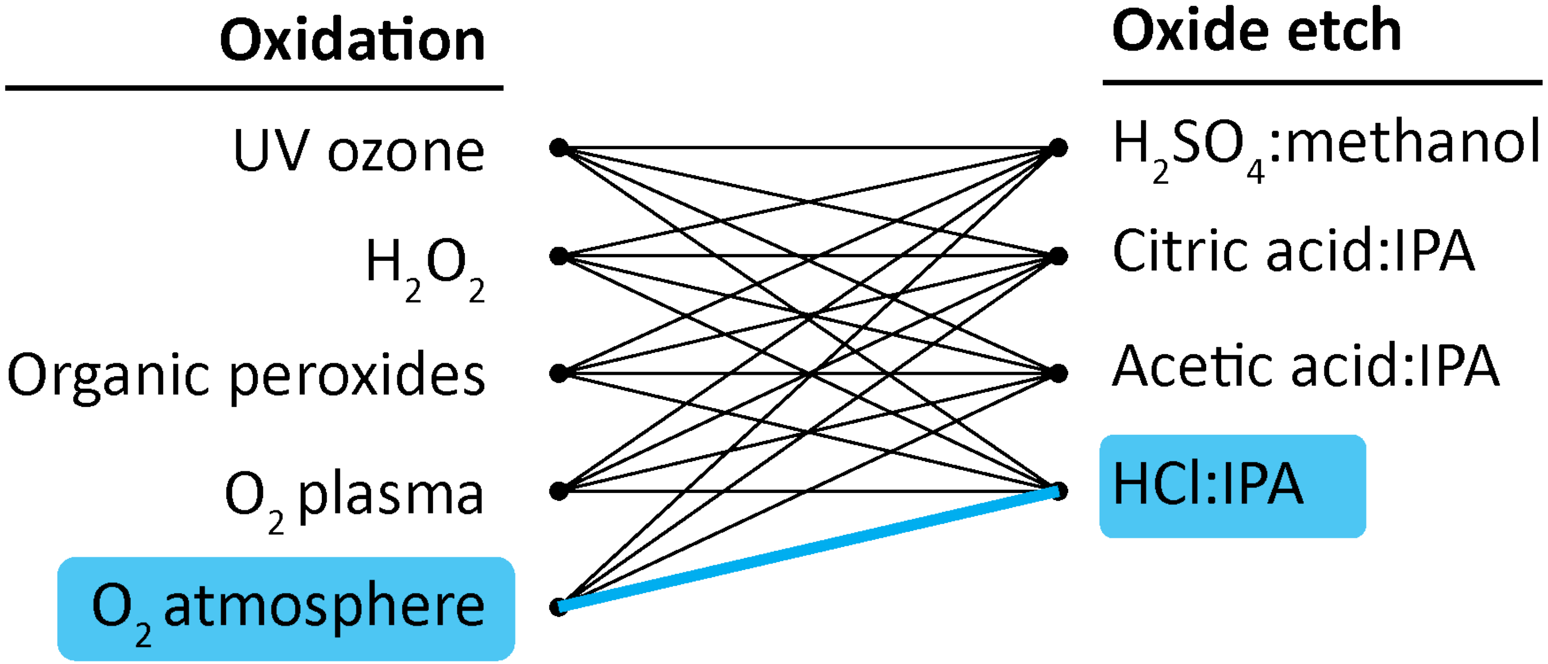
- In air:
  - Ga_2O_3, Sb_2O_3
- In strong oxidation agents:
  - Ga_2O_3, Sb_2O_3, Sb_2O_5 (insoluble in aqueous acid/alkali)

[Liu, JVST B. 2002]

DE = oxidation + dissolution, both critical for III-Sb!

III-Sb-compatible Digital Etch

Survey of digital etch combinations:



Oxidation

- UV ozone
- H_2O_2
- Organic peroxides
- O_2 plasma
- O_2 atmosphere

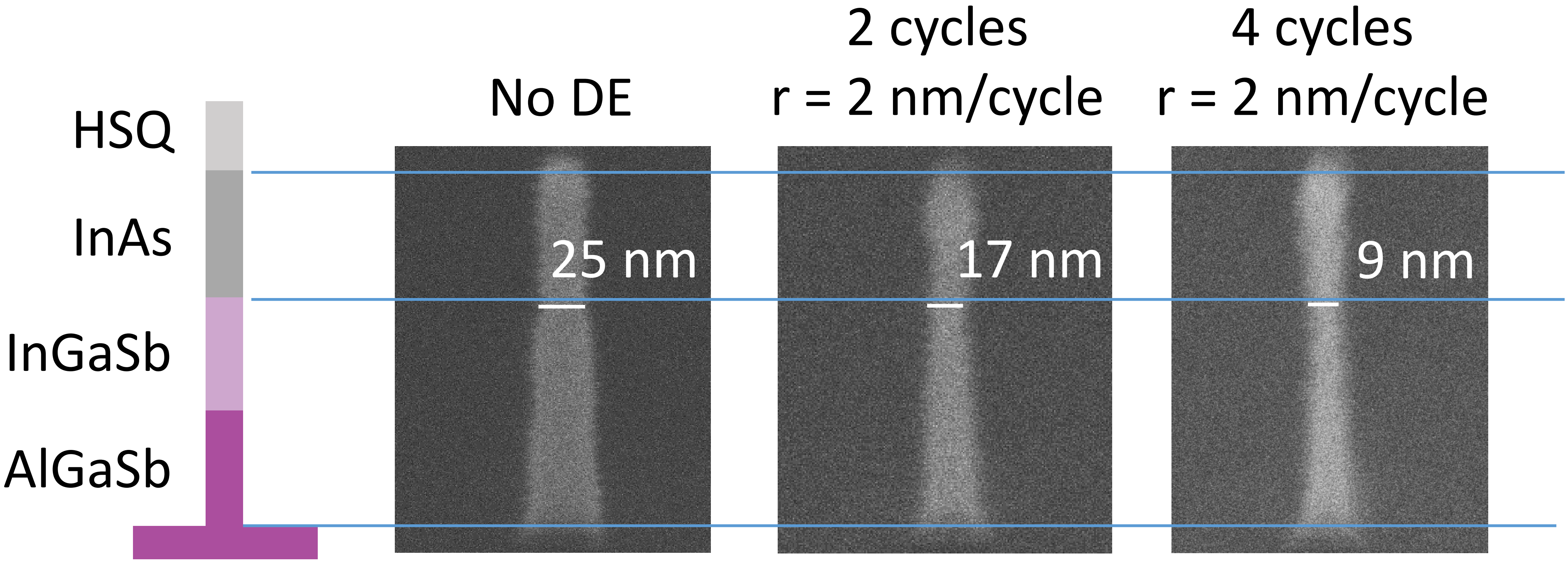
Oxide etch

- H_2SO_4:methanol
- Citric acid:IPA
- Acetic acid:IPA
- HCl:IPA

Best results: RT O_2 atmosphere + HCl:IPA

III-Sb-compatible Digital Etch

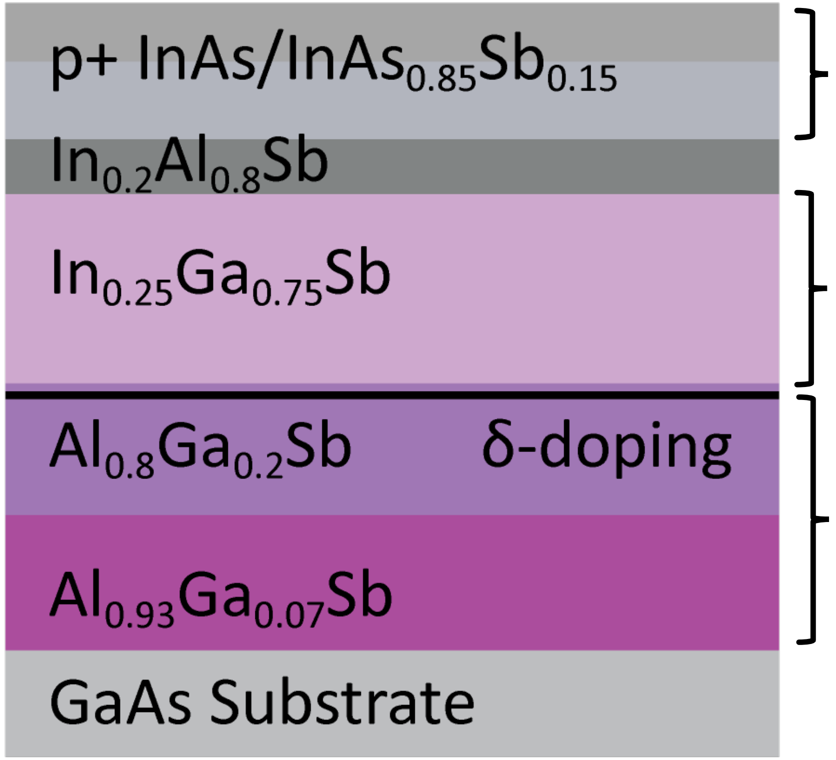
O_2 oxidation + HCl:IPA, IPA rinsing



r (III-As) = r (III-Sb)

InGaSb FinFETs

Heterostructure (MBE at KIST)



p+ $InAs/InAs_{0.85}Sb_{0.15}$

$In_{0.2}Al_{0.8}Sb$

$In_{0.25}Ga_{0.75}Sb$

$Al_{0.8}Ga_{0.2}Sb$ δ-doping

$Al_{0.93}Ga_{0.07}Sb$

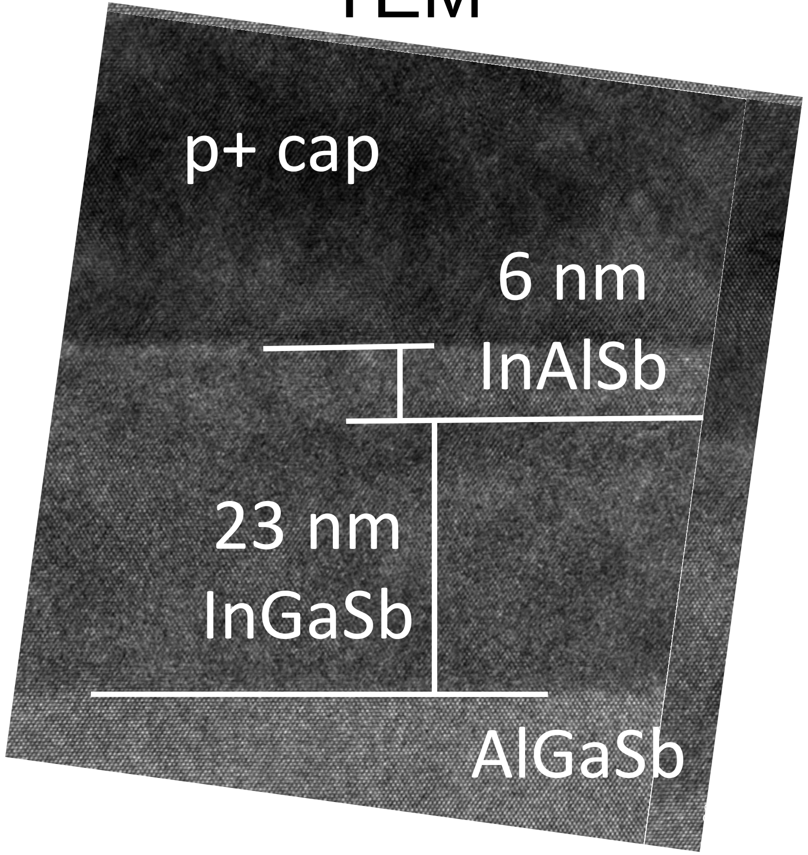
GaAs Substrate

Composite cap

-1.1% strain
H_c = 23 nm

Graded buffer

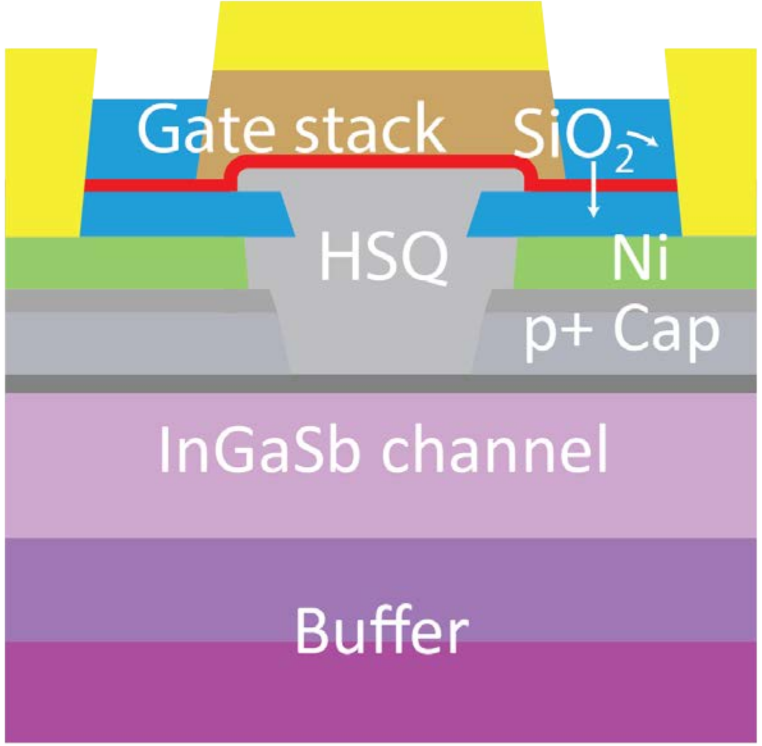
TEM

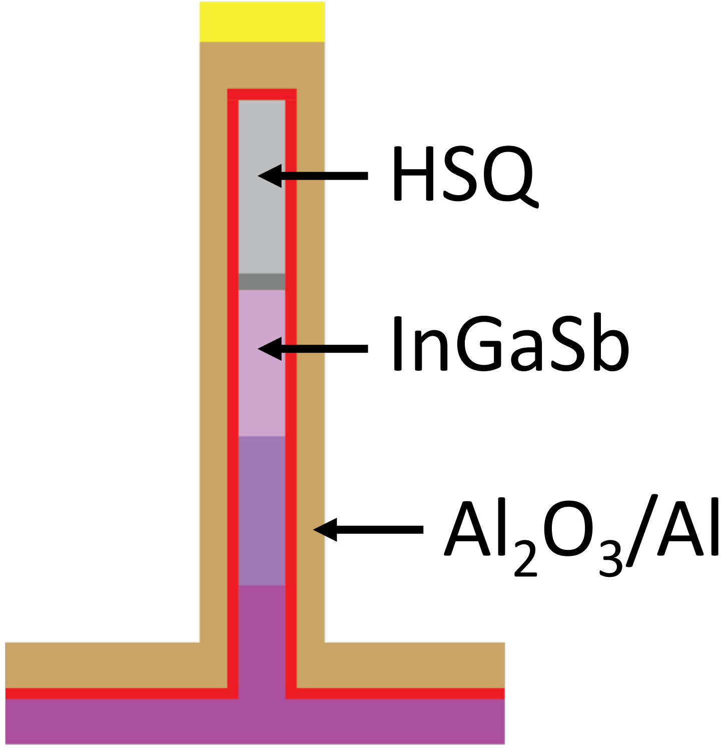


- Channel $\mu_p = 1175\ cm^2/V{\cdot}s$
- Buffer/channel resistivity ~ 10^9

InGaSb FinFET Process

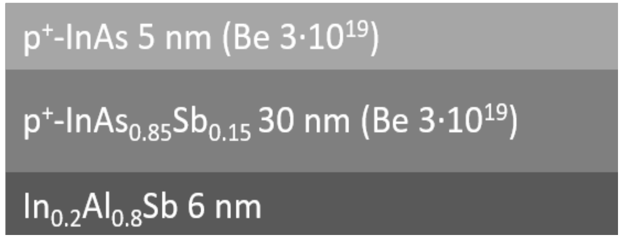
- Ni Ohmic contact
- SiO_2 spacer
- Gate recess (dry + wet)
- Fin RIE
- Digital etch
- Al_2O_3/Al Gate stack
- Via + metal





Ohmic Contacts

Ni contacts, 350 °C RTA, 3 min

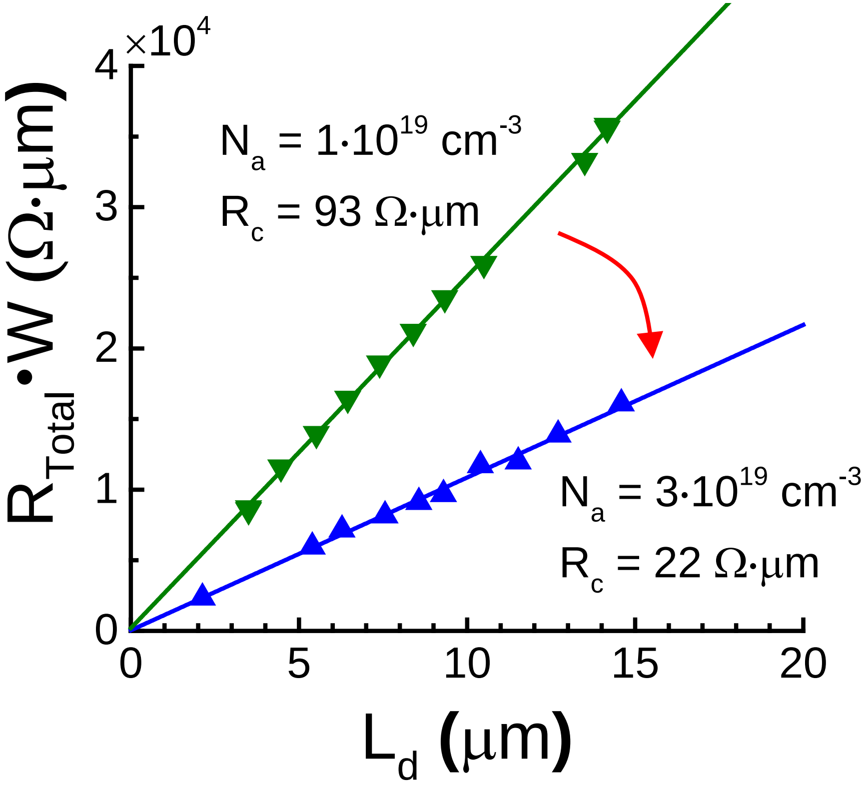


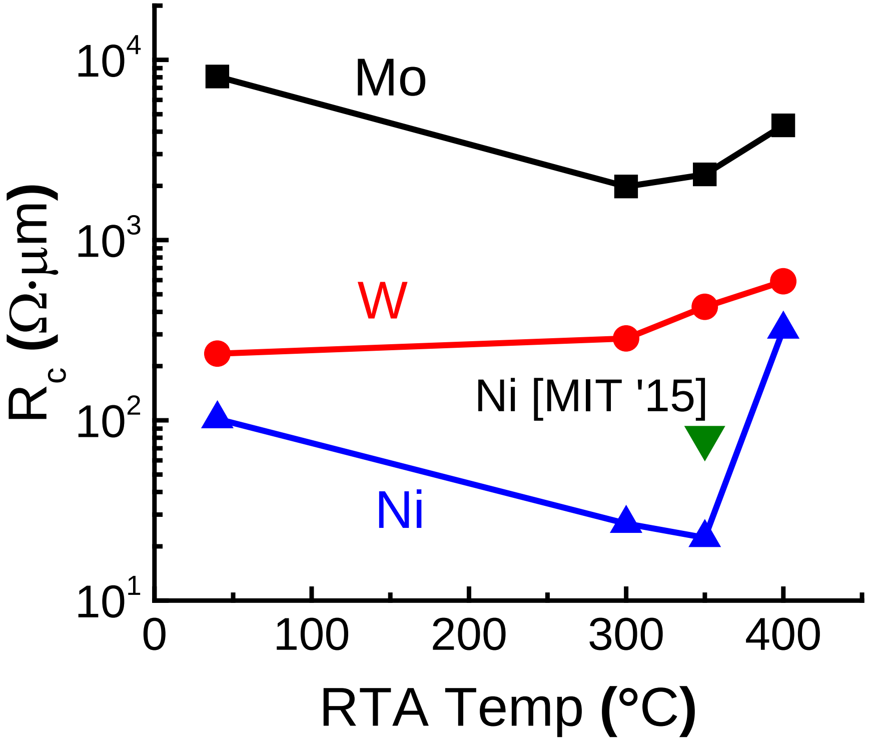
p^+-InAs 5 nm (Be $3\cdot10^{19}$)

p^+-InAs$_{0.85}$Sb$_{0.15}$ 30 nm (Be $3\cdot10^{19}$)

In$_{0.2}$Al$_{0.8}$Sb 6 nm

[Guo, EDL, 2015]

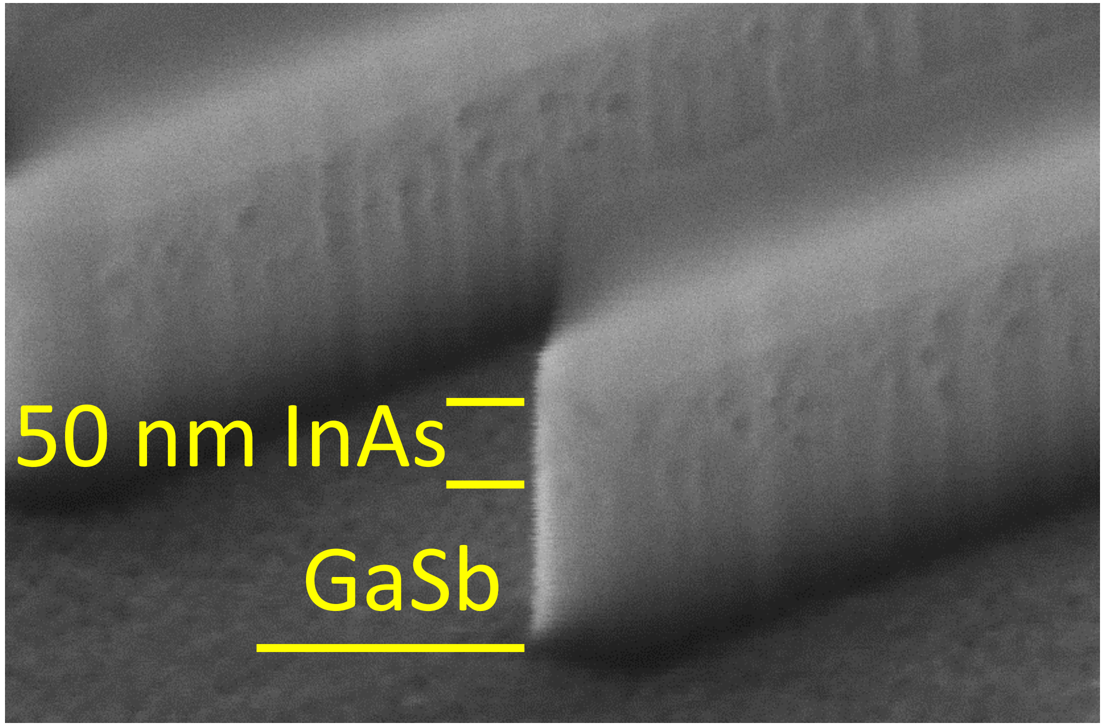




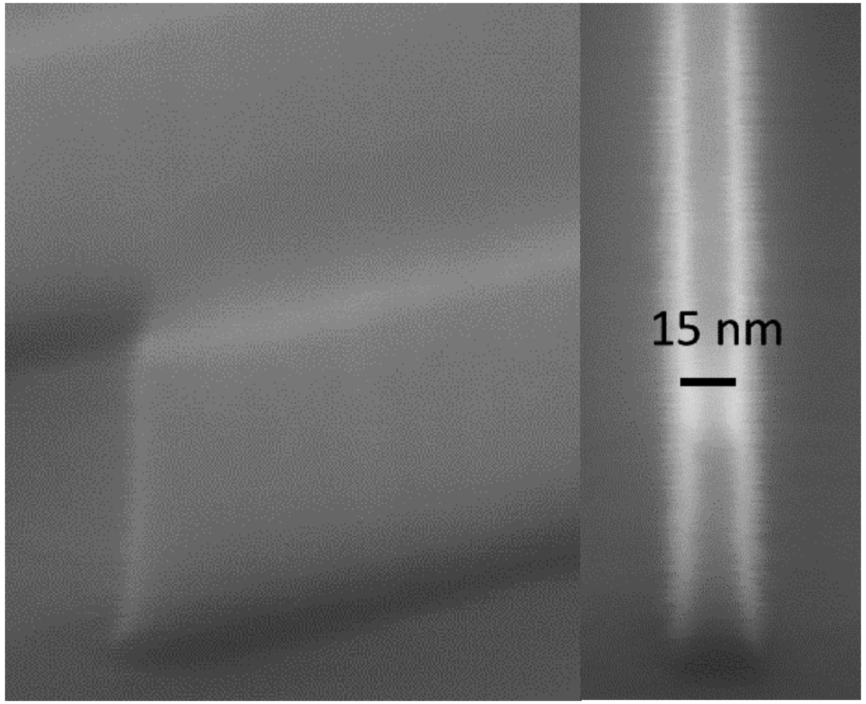
R_c = 22 Ω·µm → 4x reduction of R_c from 2015 FinFETs

Fin Etch

BCl_3/N_2 13.5:5.5, 250°C
[Lu, IEDM 2015]



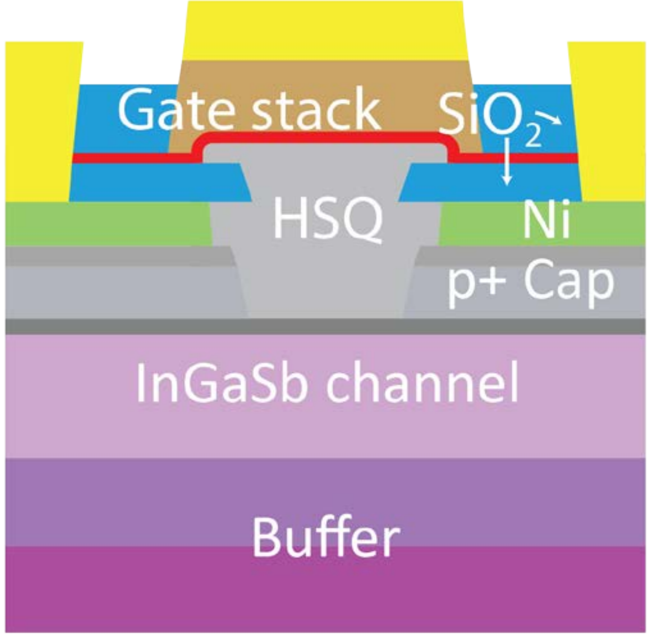
$BCl_3/Ar/SiCl_4$ 3:11:0.4, 250°C
This work

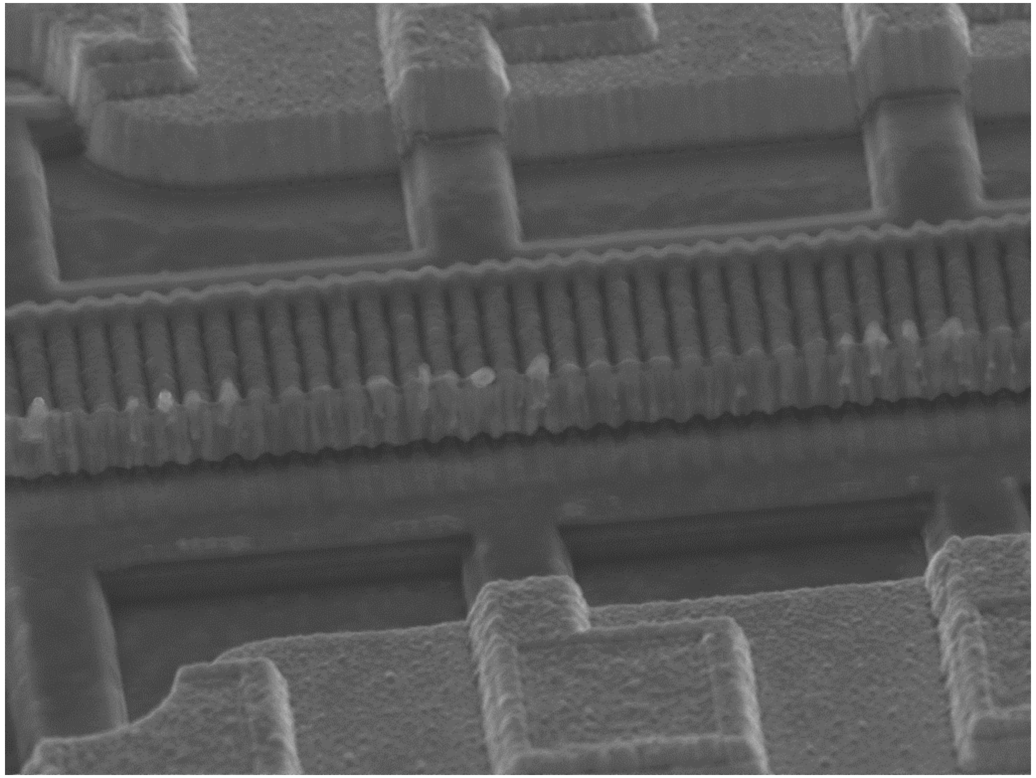


High-quality simultaneous InAs and GaSb etching

InGaSb FinFET Process

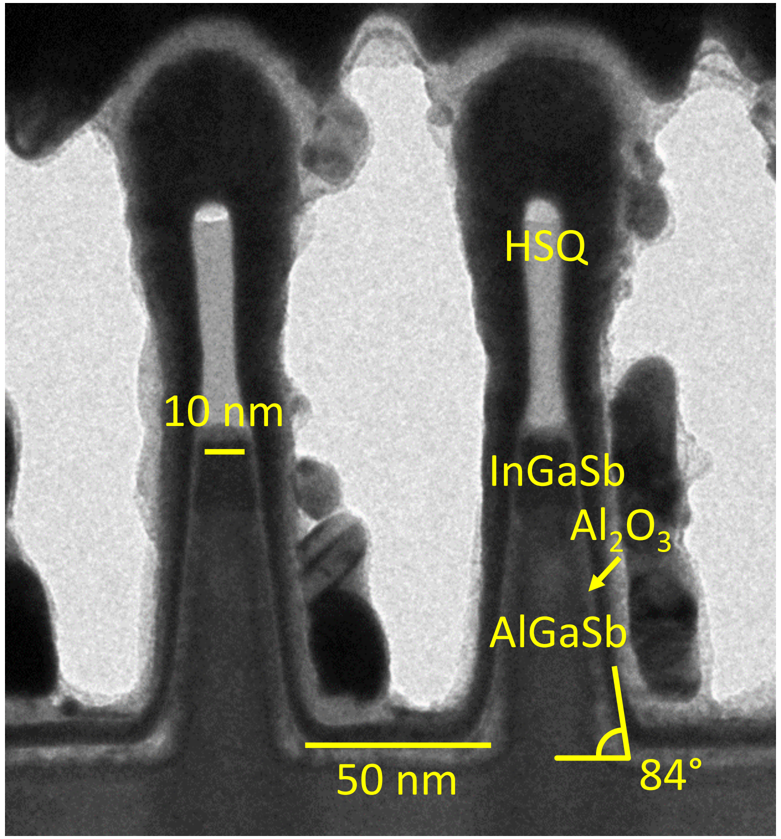
Finished devices

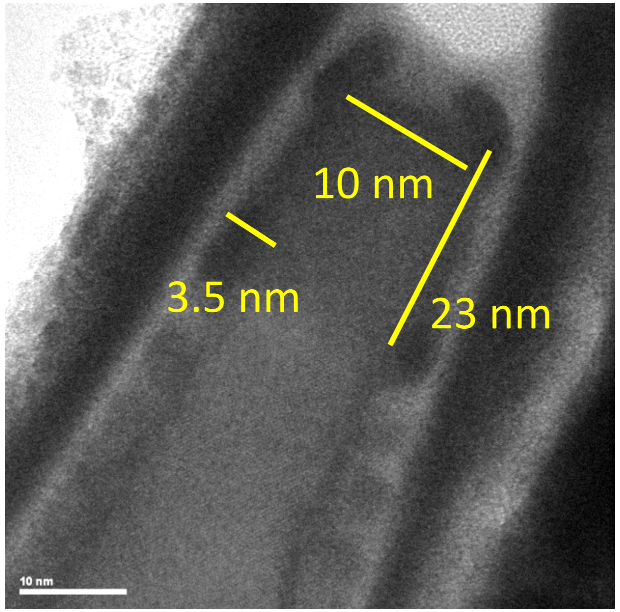




- 3.5 nm Al_2O_3 gate dielectric
- Final FGA anneal at 150 °C for 3 min

InGaSb FinFET Process

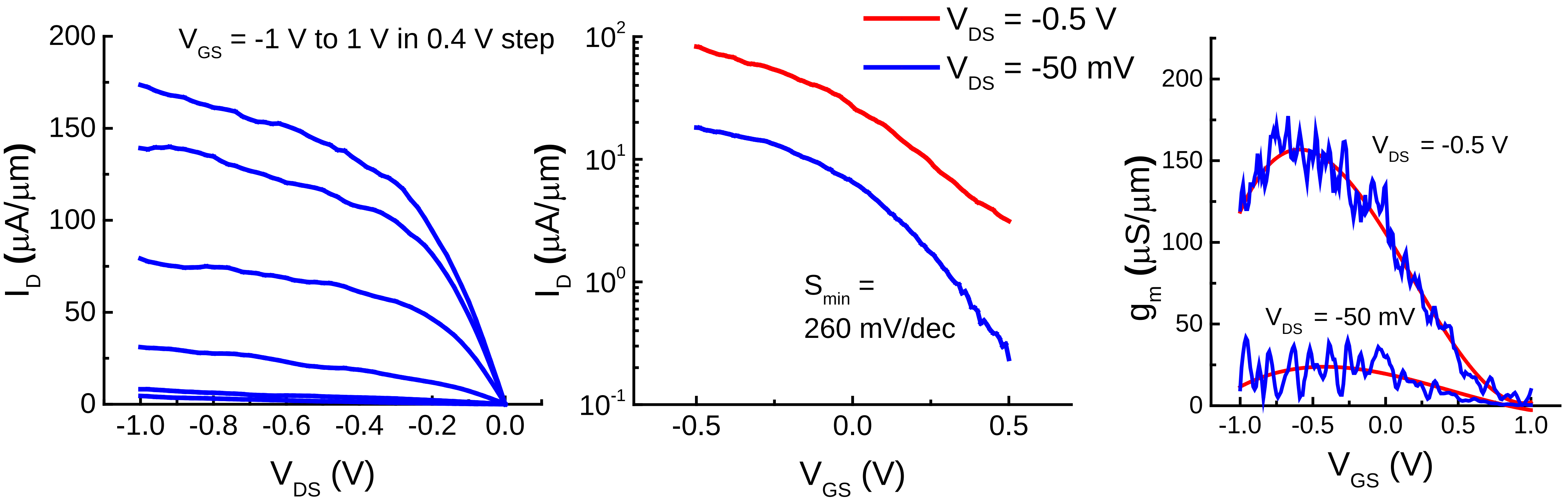




- Narrowest W_f = 10 nm
- Fin AR = 2.3

Electrical Characteristics

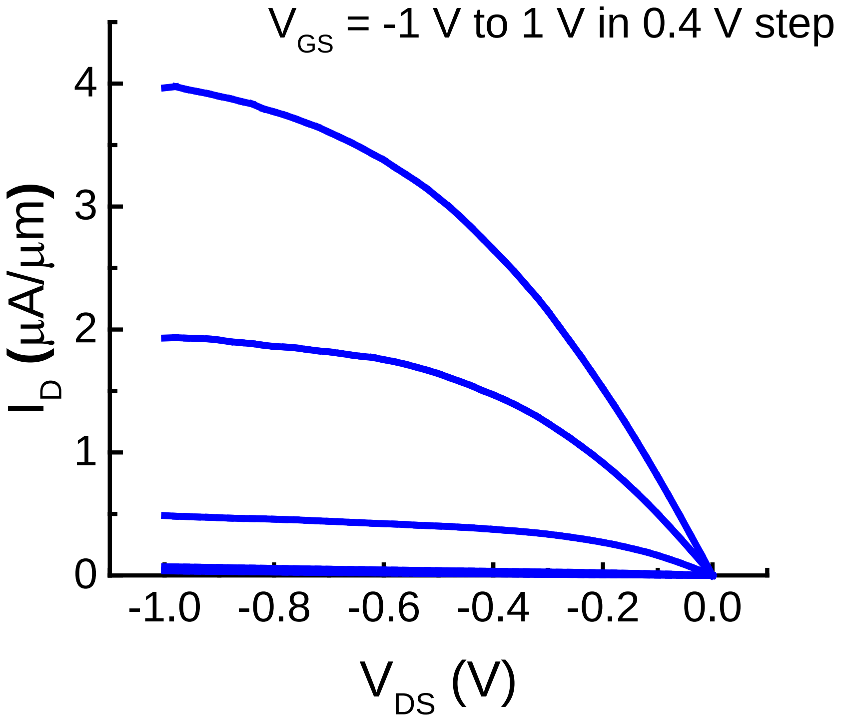
$W_f = 10$ nm, $L_g = 20$ nm, $N_f = 1$

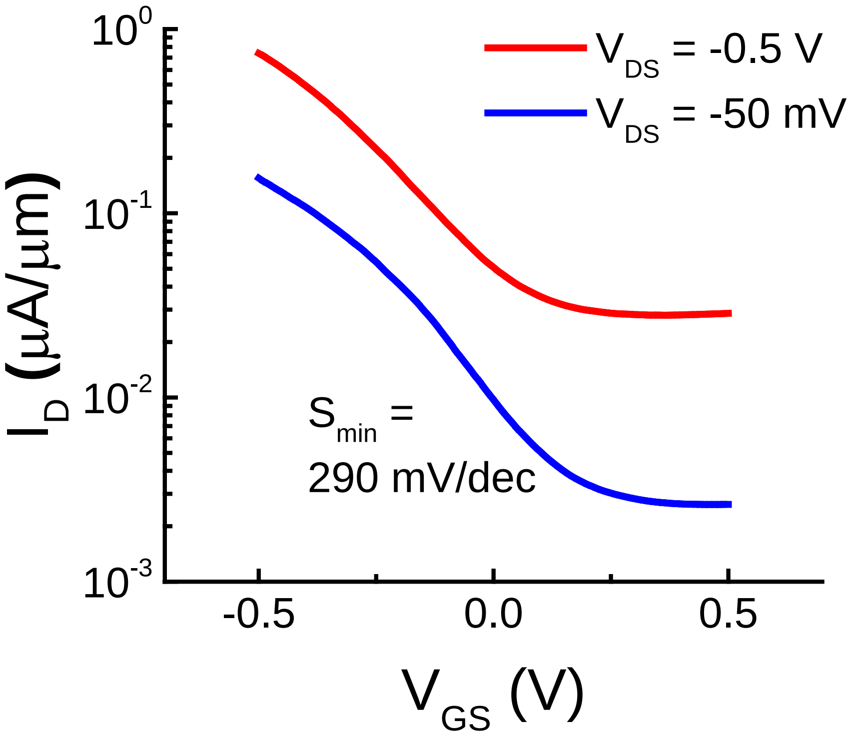


- S ~ 260 mV/dec
- $g_{m,max}$ = 160 µS/µm
- Single fin device: current fluctuations

Electrical Characteristics

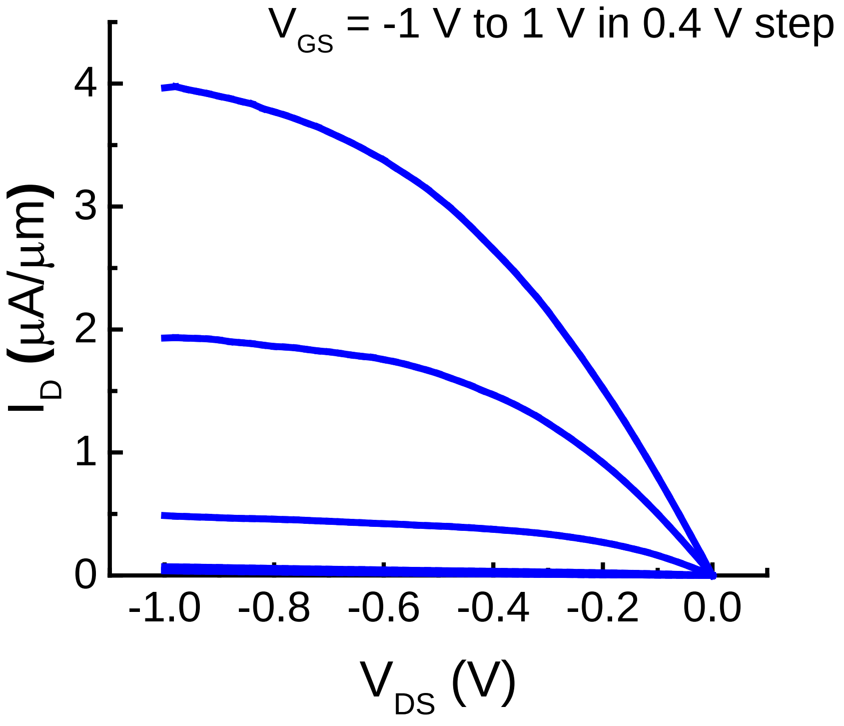
W_f = 10 nm, L_g = 1 µm, N_f = 100



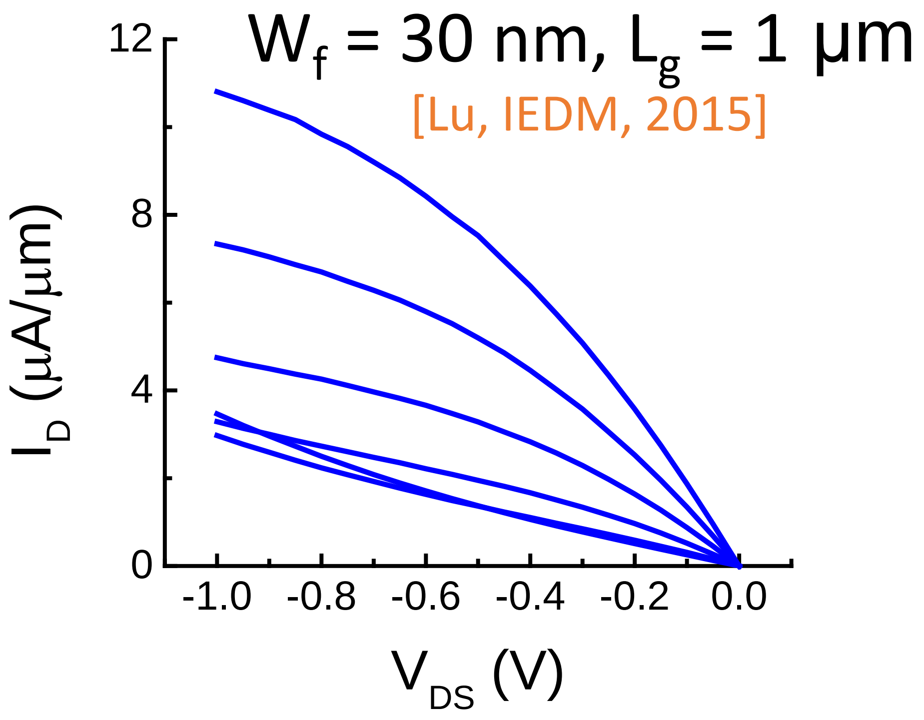


Electrical Characteristics

W_f = 10 nm, L_g = 1 μm, N_f = 100



V_{GS} = -1 V to 1 V in 0.4 V step

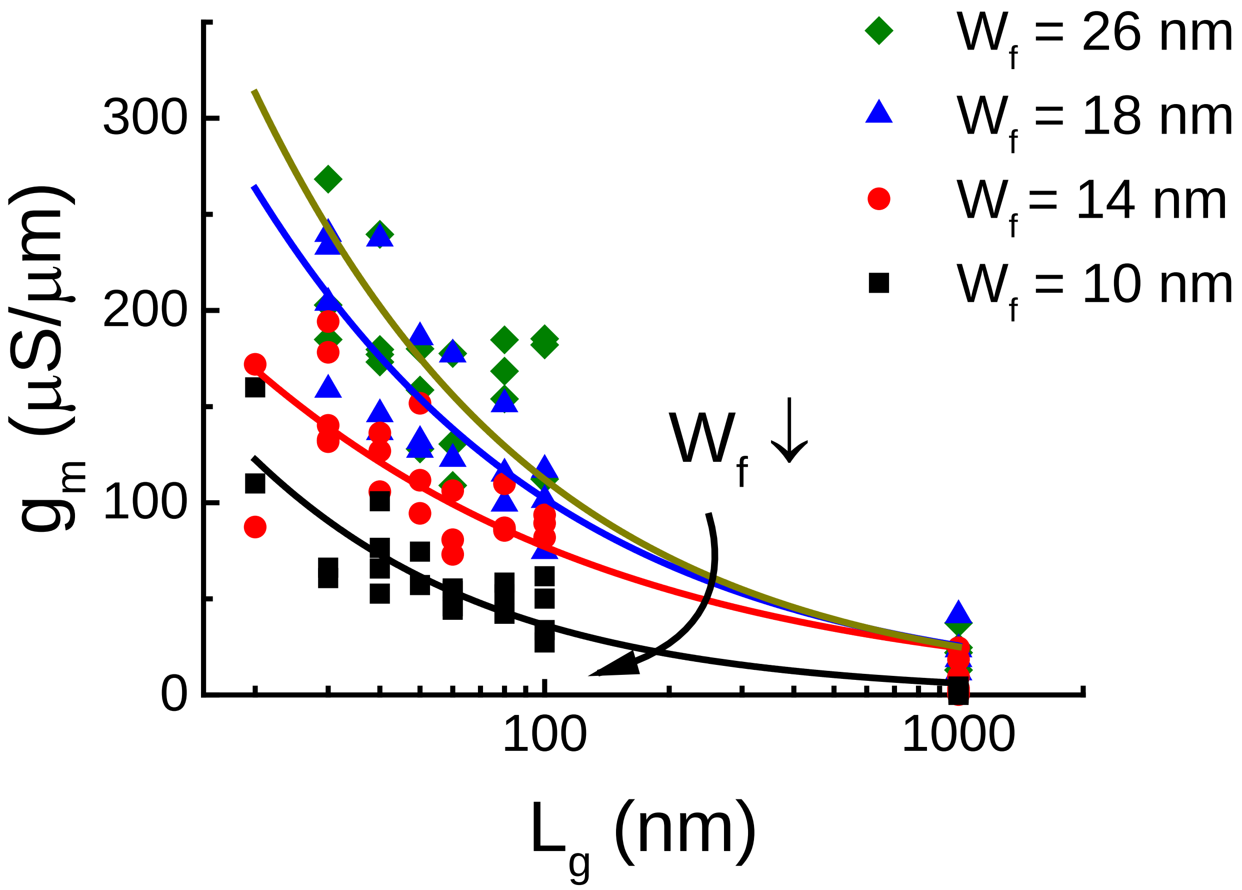


W_f = 30 nm, L_g = 1 μm

[Lu, IEDM, 2015]

Significant improvement over 1st gen FinFETs

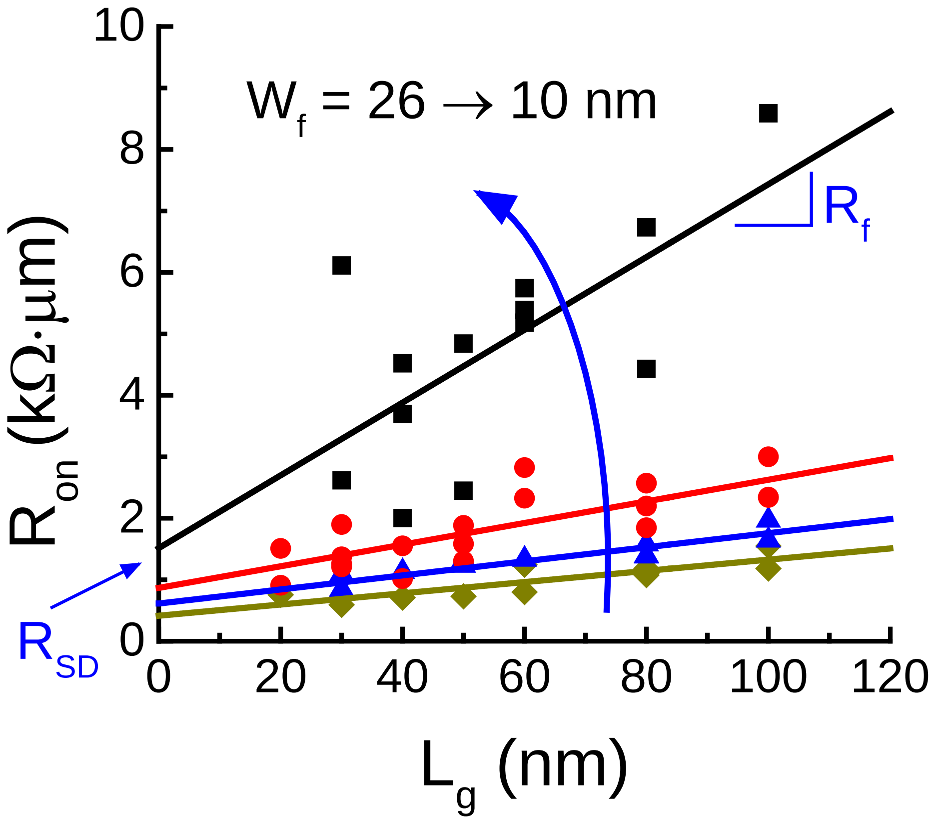
g_m Scaling



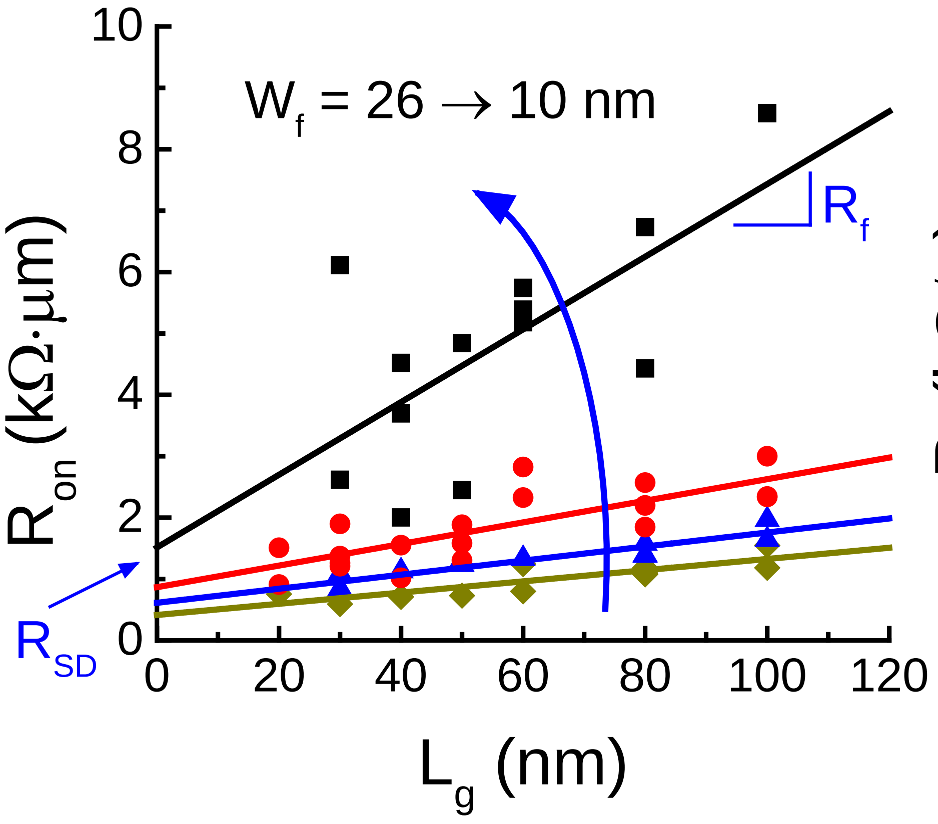
L_g ↓ → g_m ↑

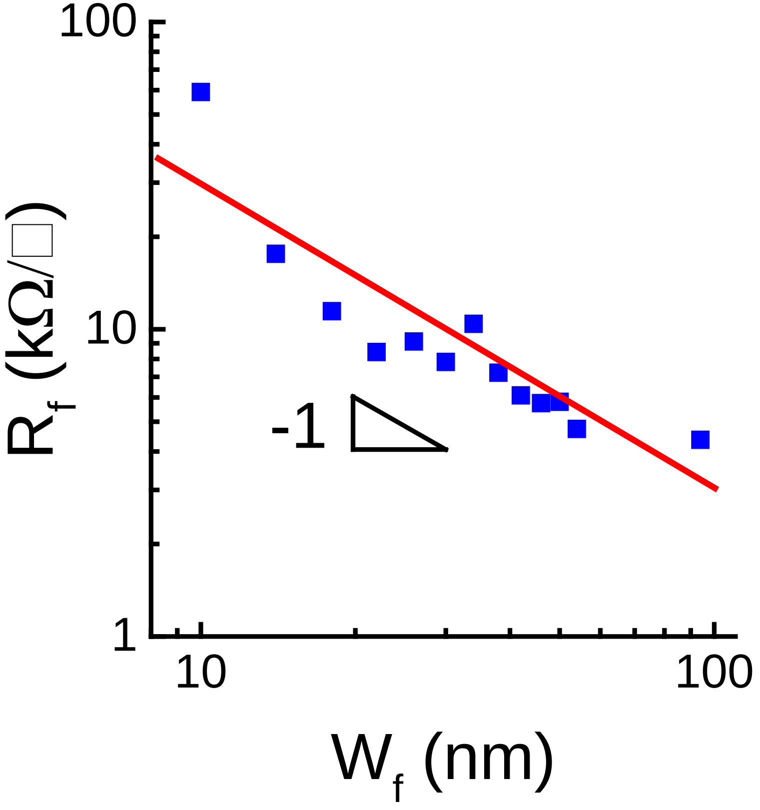
W_f ↓ → g_m ↓

ON Resistance

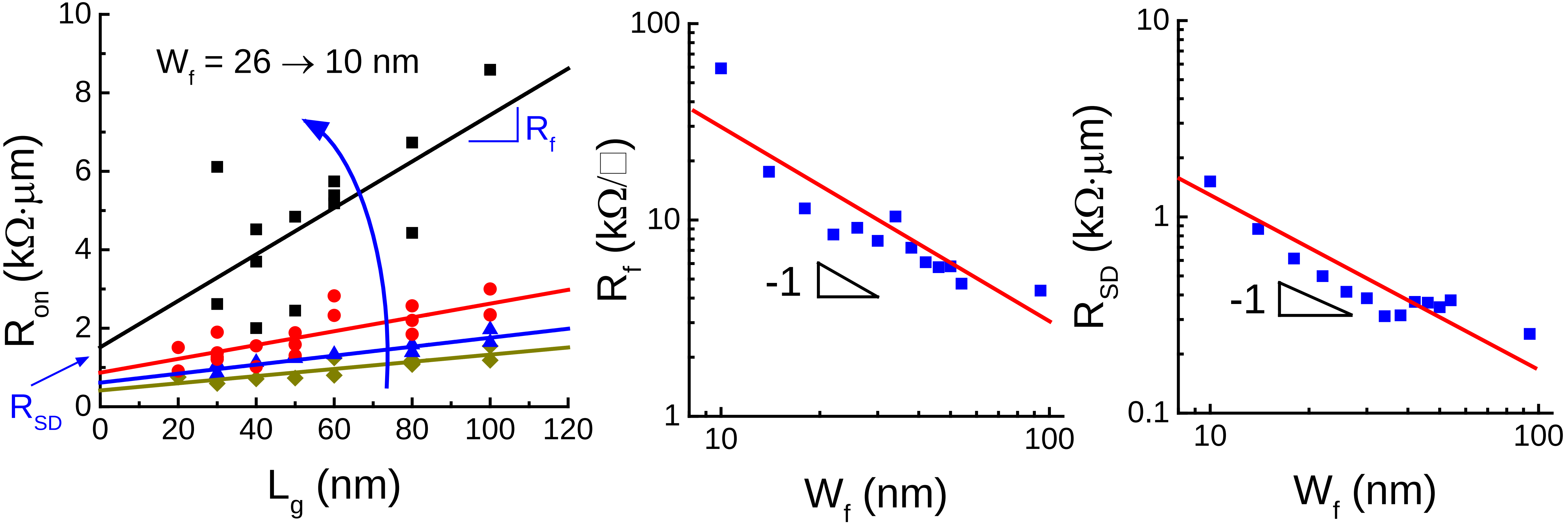


ON Resistance



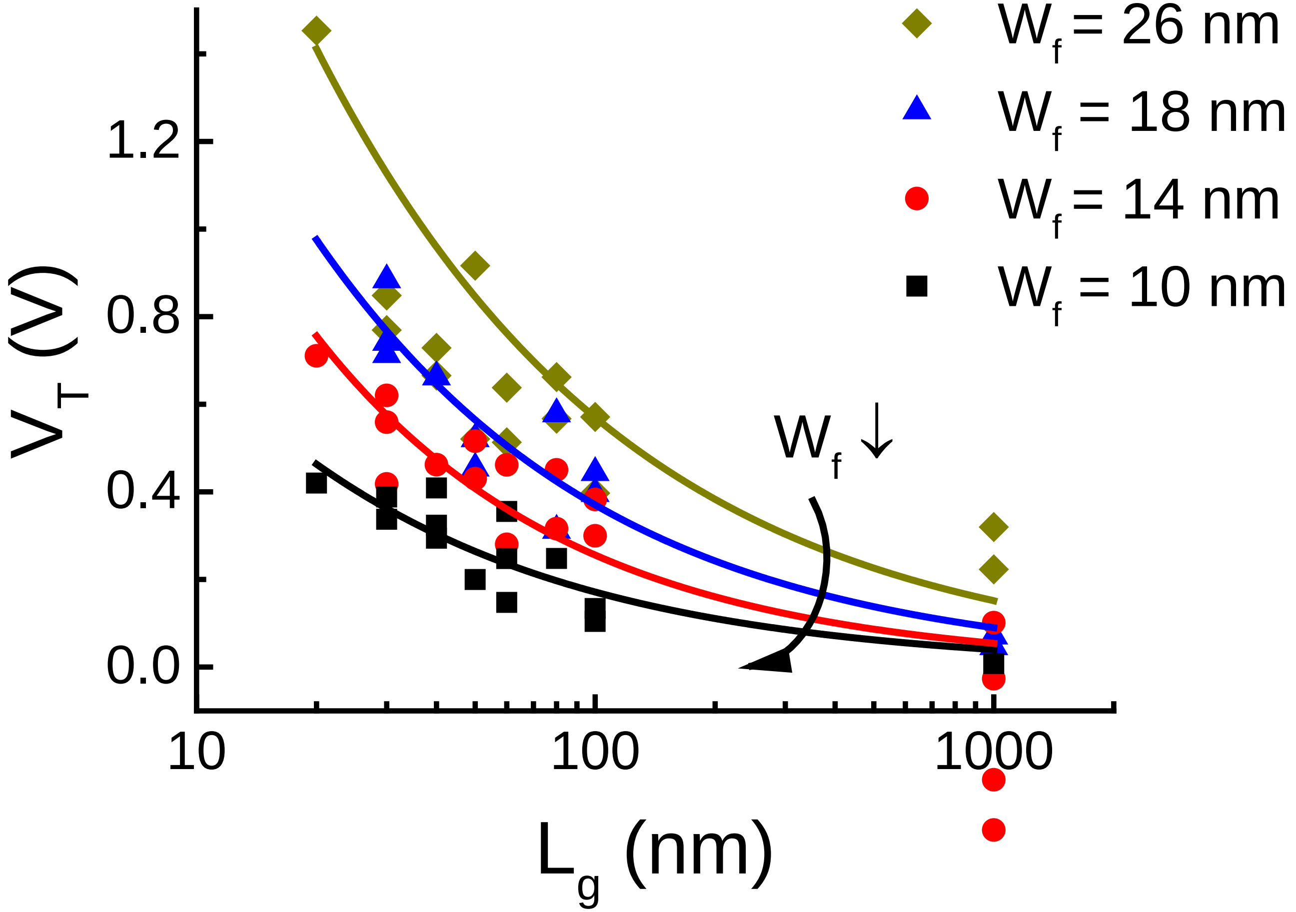


ON Resistance



R_f and R_{SD} ~ $1/W_f$

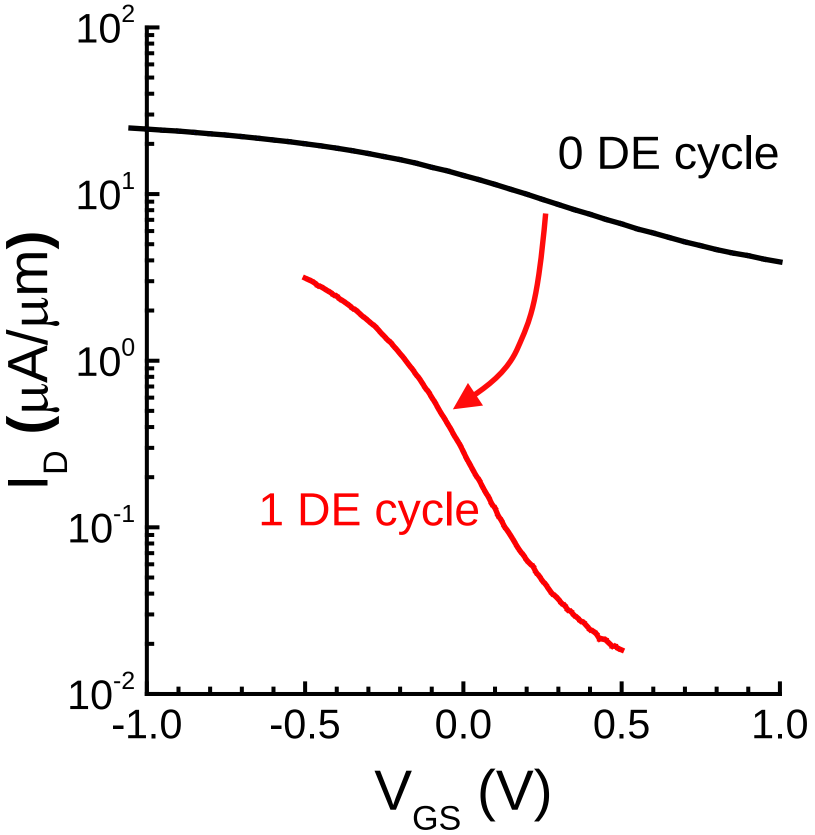
V_T Scaling



W_f ↓ → better V_T roll-up

Off-state Current

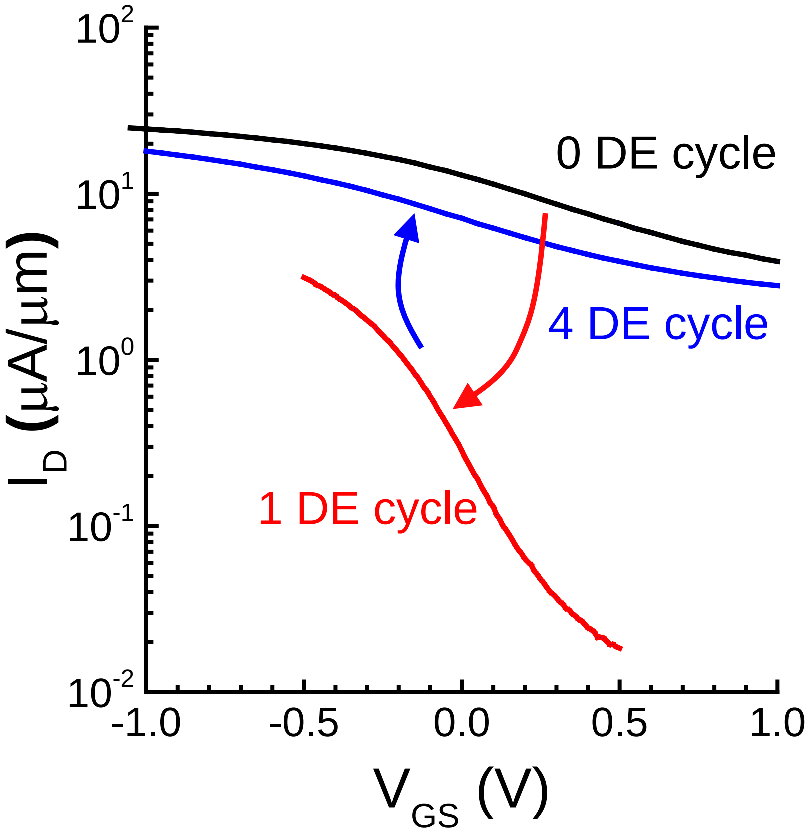
W_f = 20 nm, L_g = 1 µm



1 DE cycle significantly improves off current

Off-state Current

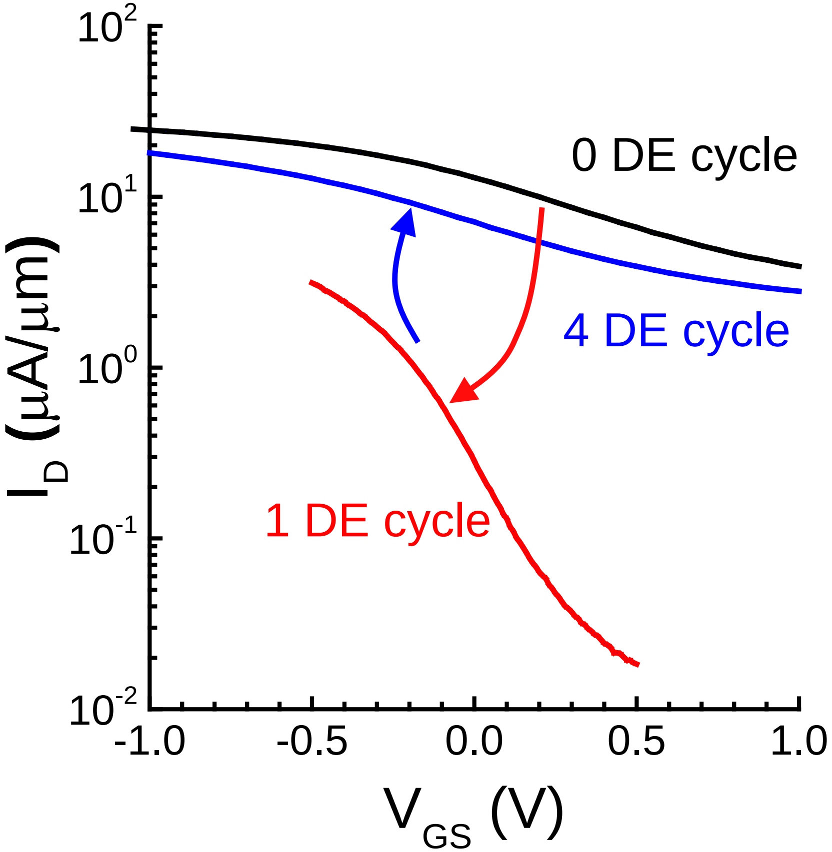
W_f = 20 nm, L_g = 1 µm



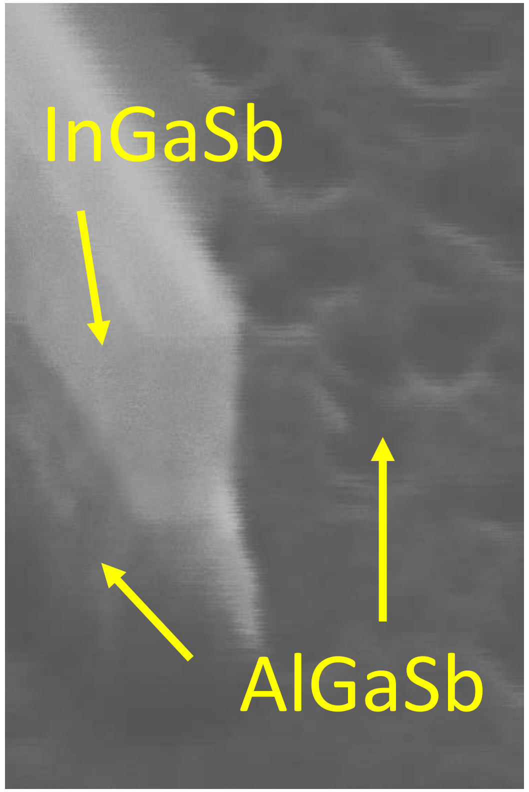
Device degrades after multiple DE cycles

Off-state Current

W_f = 20 nm, L_g = 1 µm



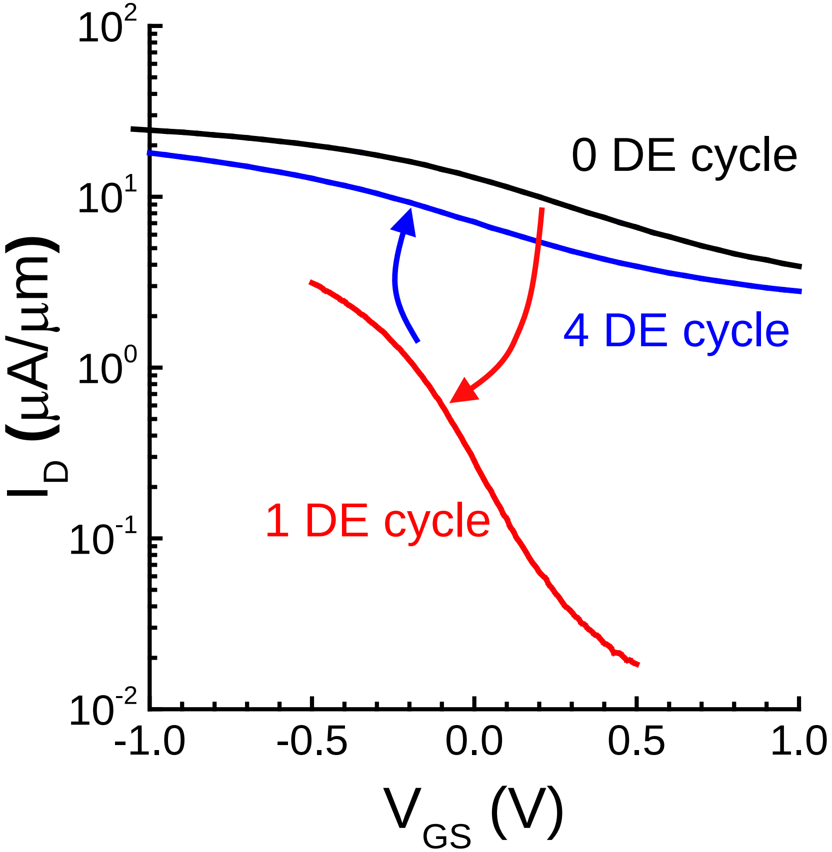
3 cycles of DE



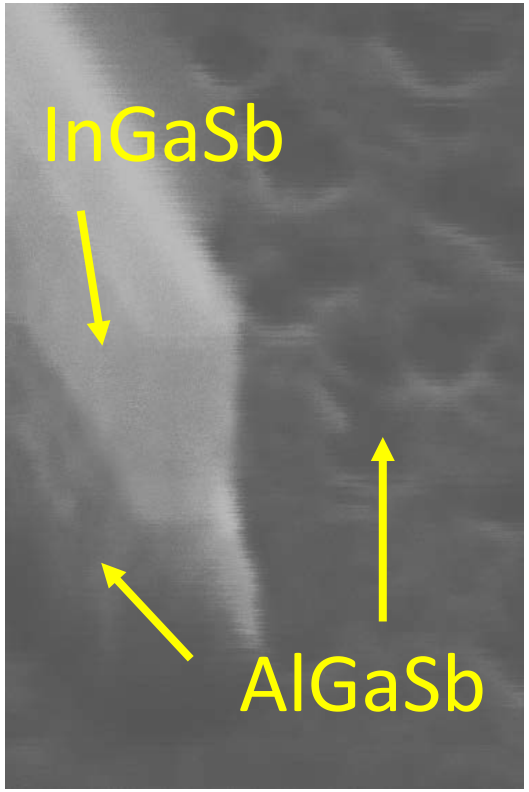
- Buffer is damaged after multiple DE cycles

Off-state Current

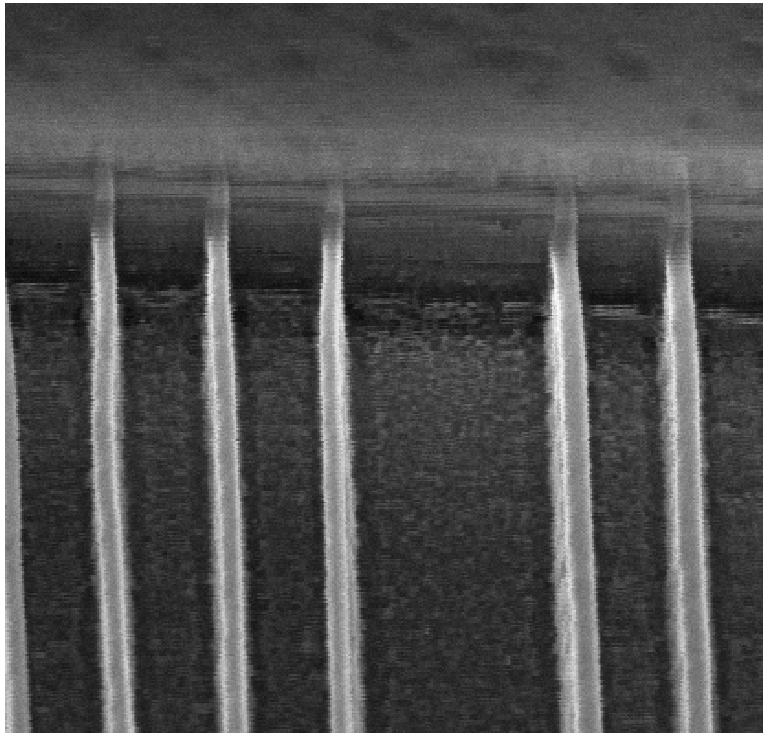
W_f = 20 nm, L_g = 1 µm



3 cycles of DE

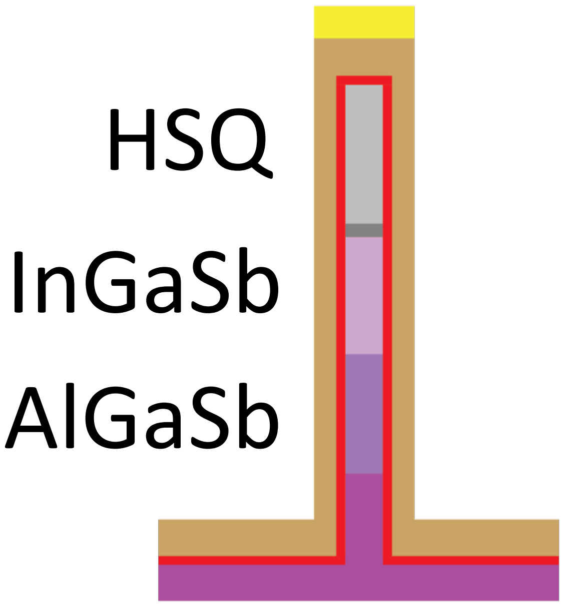


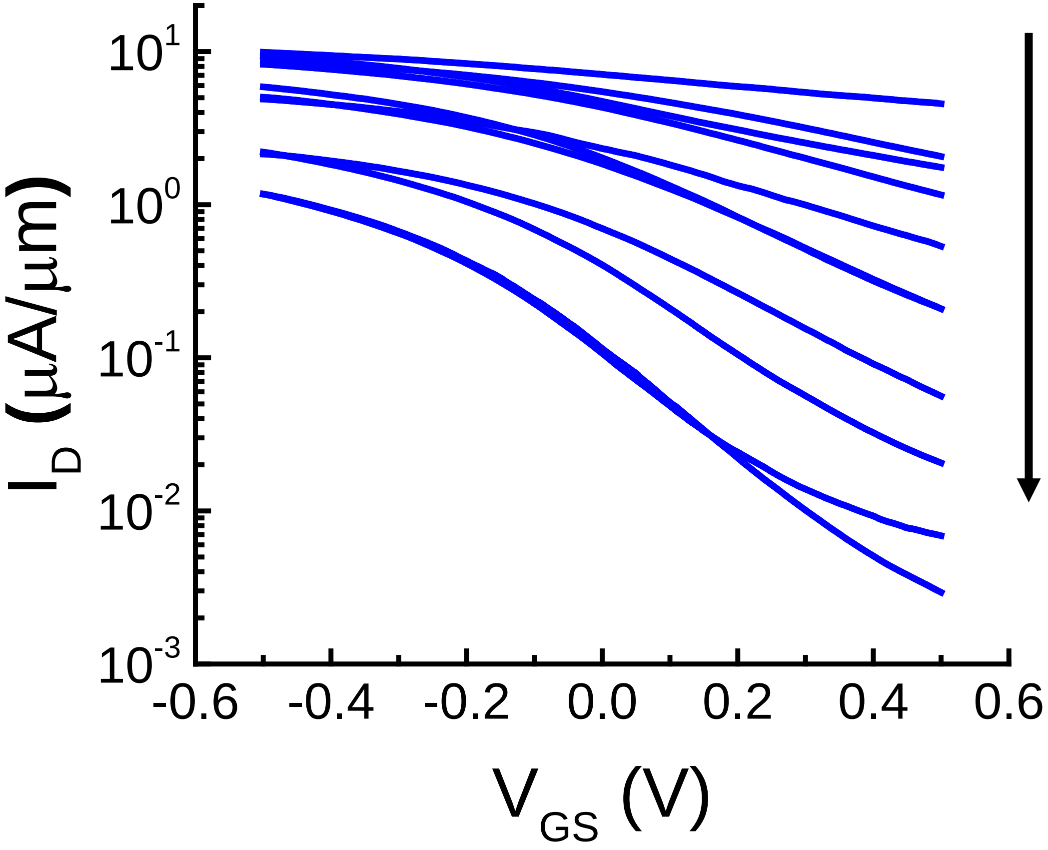
Exposure in air after fin etch



- Buffer is damaged after multiple DE cycles
- AlGaSb is very reactive

Off-state Current

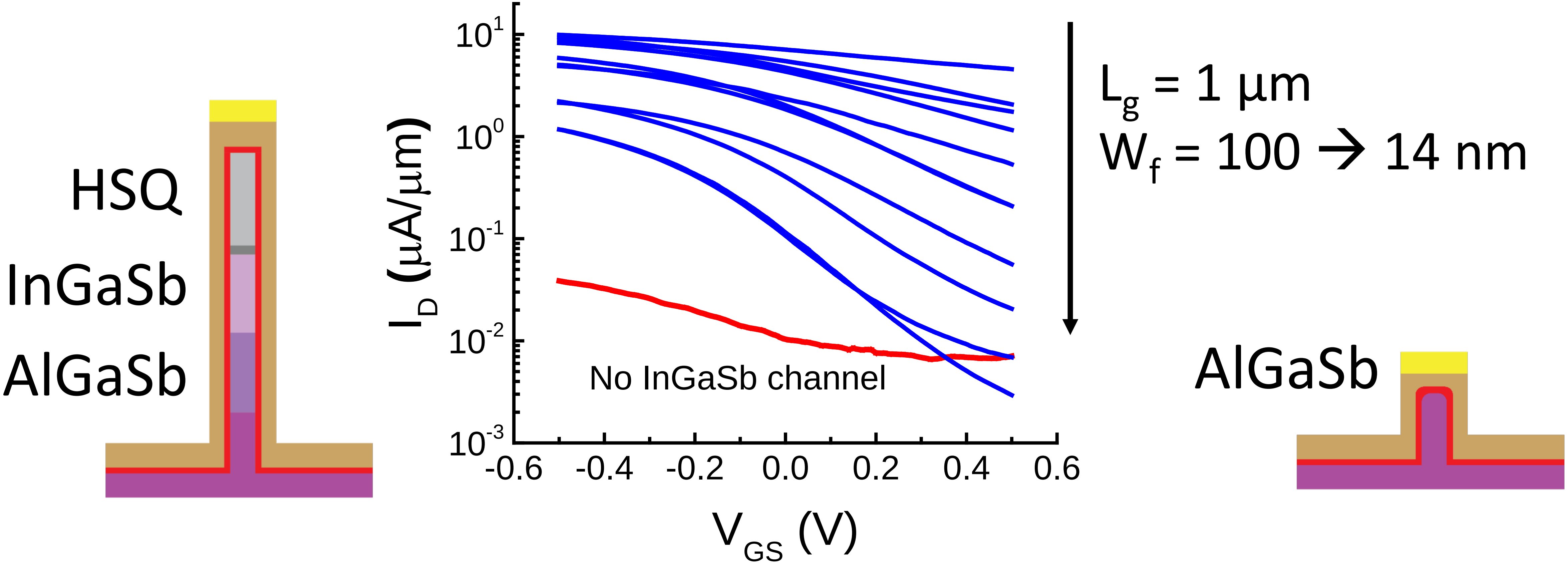




L_g = 1 µm

W_f = 100 → 14 nm

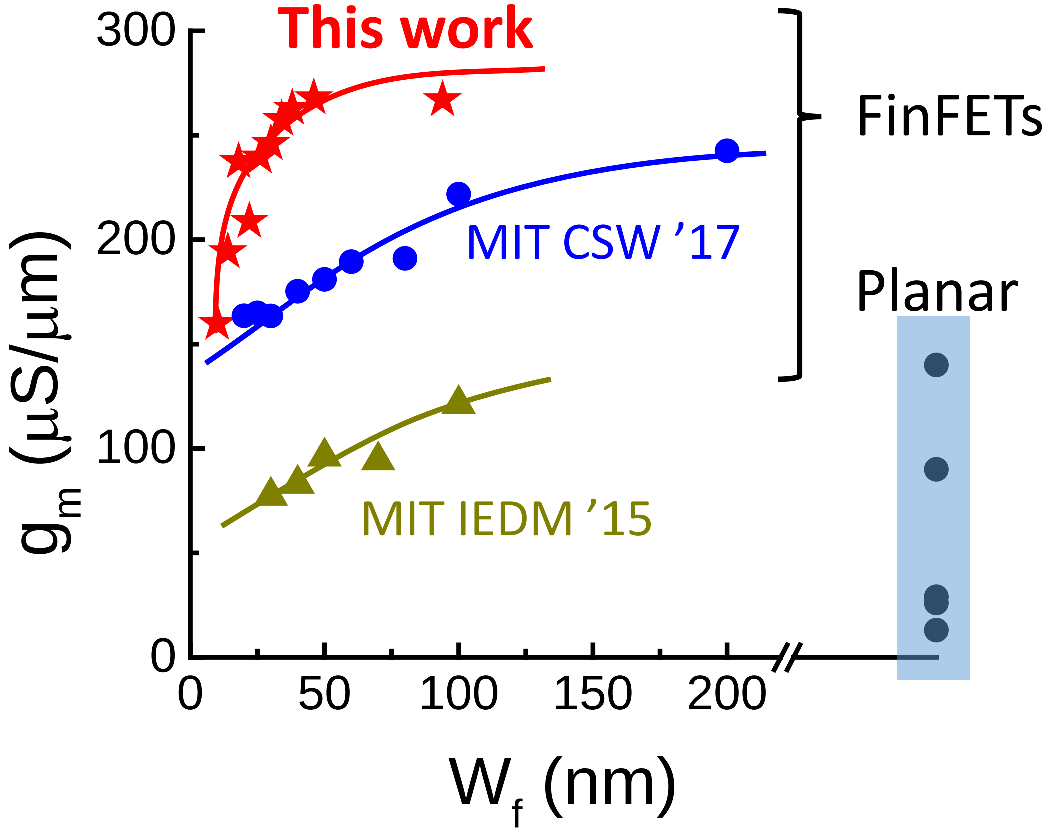
Off-state Current



Buffer leakage contributes substantially to off current

Benchmark

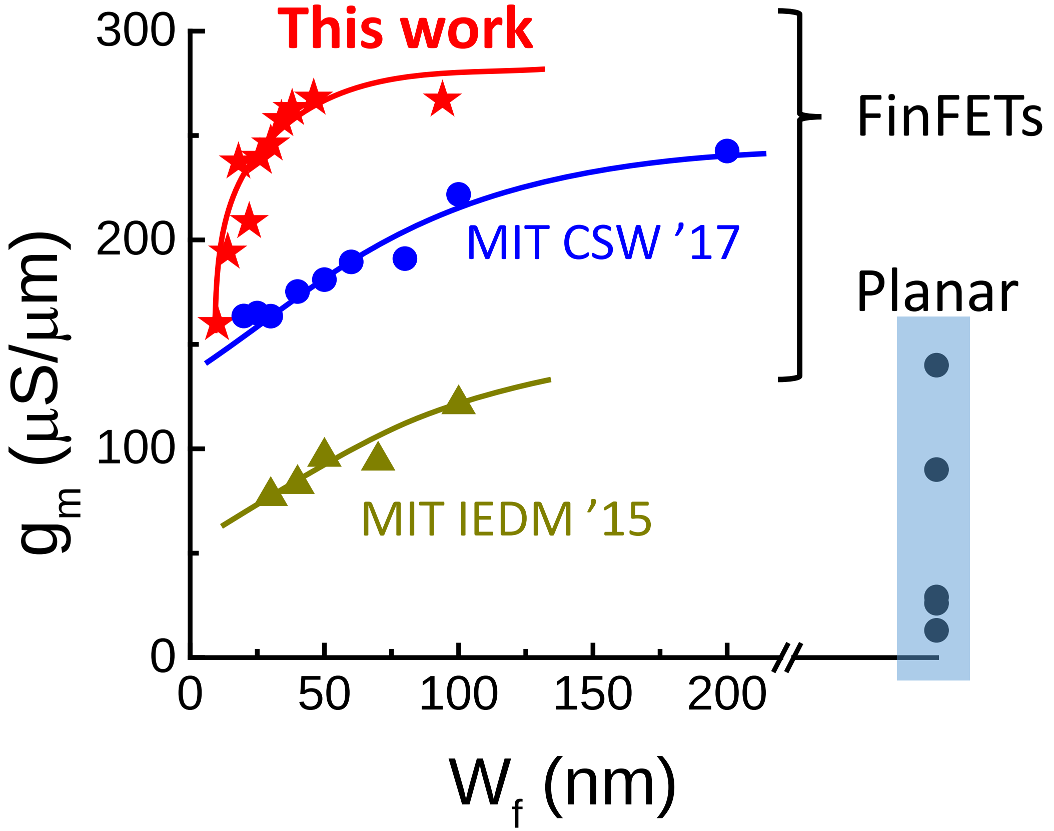
Normalized by conducting width



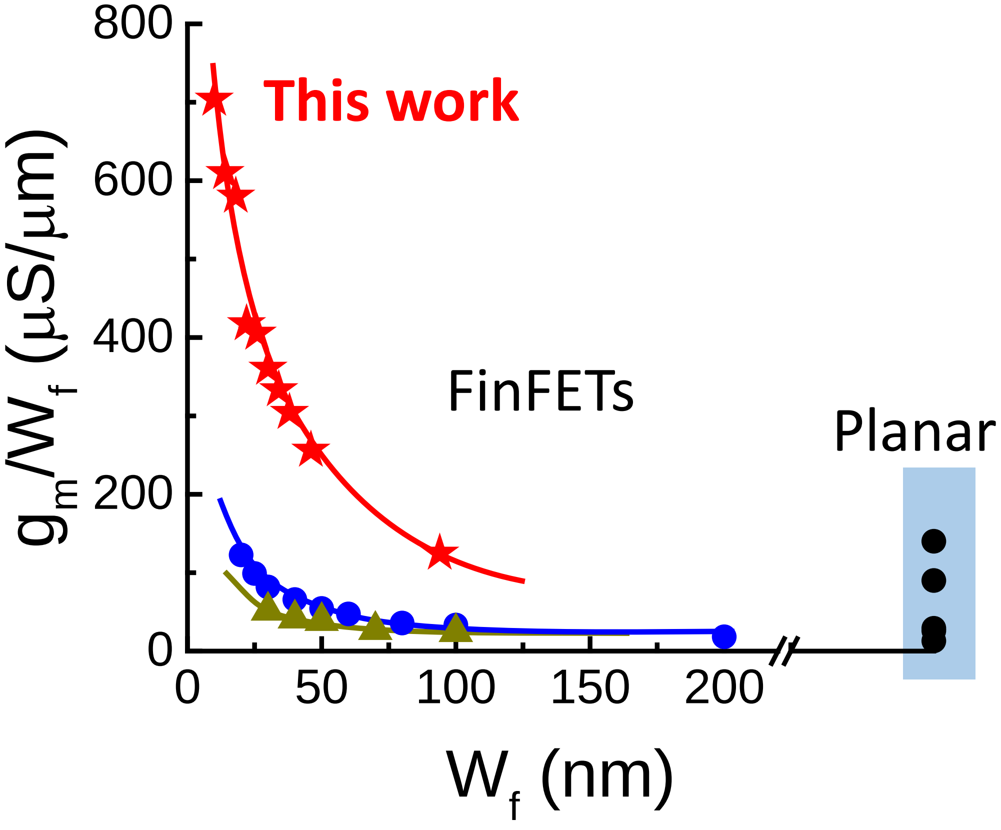
Record g_m = 268 µS/µm at W_f = 46 nm

Benchmark

Normalized by conducting width



Normalized by W_f



If normalized by footprint, g_m = 704 µS/µm at W_f = 10 nm

Conclusions

- Studied sidewall cleaning of InGaSb FinFETs
  - III-Sb-compatible digital etch
  - Etching rate = 2 nm/cycle
  - Mitigation of surface leakage
- Demonstrated most scaled InGaSb p-channel FinFETs
  - Minimum W_f = 10 nm
  - Record device performance
  - Improved subthreshold performance
- Face challenge: to improve turn-off characteristics